APPLICATION NOTE ANP25

PowerBlox™ Thermal Analysis

Introduction

The primary factor limiting how much current a PowerBlox™ device can deliver is heat. Heat is generated by losses in the PowerBlox™ package and comes from four main sources: conduction Losses in the FETs, switching losses in the FETs and FET drivers, losses in the internal LDO, and losses in the controller required to run the power supply. Another loss that can be significant is the power lost in the output inductor DCR. The ability of the PowerBlox™ devices to dissipate heat will be closely examined in this report.

Description of Testing Completed

Three PowerBlox™ configurations were tested:

A) SP7662 on a 4 layer PCB with a layout having components on one side
B) SP7662 on a 4 layer PCB with a layout having components on two sides
C) SP7655 on a 4 layer PCB with a layout having components on two sides and an increased via count

Each power supply was configured for 12Vin and 3.3Vout. An airflow chamber that could provide temperature regulated laminar airflow was used to create consistent test conditions. Each unit was monitored using an Infrared Thermal camera to record temperature levels and thermal images. The power input, output, and dissipation was measured for a variety of conditions to create power derating curves for each device. While this is useful for the particular input/output/inductor configuration, a more generic power dissipation derating curve was created that will serve as a guideline to any PowerBlox™ application.

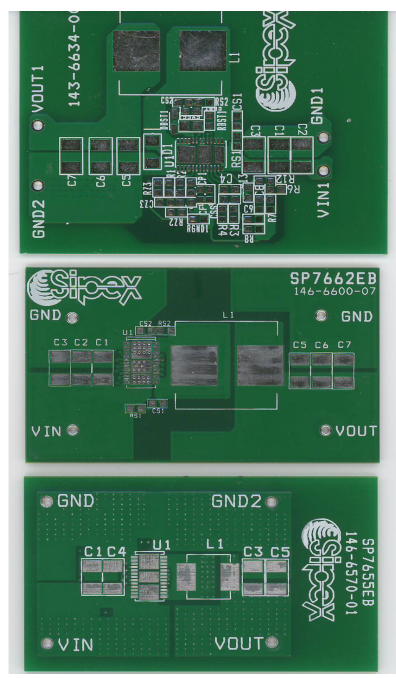
Comparison of PCBs Used

The construction of each PCB is the same, standard FR4 type material. All traces on inner and outer layers are 2 ounce copper. All the PCBs will be examined in greater detail within the report.

PCB A: Single Sided – No Vias. This 4 layer PCB is the SP766x evaluation board for customers wanting a solution having components only on one side. Adding no thermal vias also means the PCB uses the minimum of board space on the back side.

PCB B: Double Sided – Multiple Vias. This 4 layer board is the SP7662 standard evaluation board. This PCB has a total of 28 vias under the part. It also has larger areas of copper for the PowerBlox™ to sink heat into. The layout places components on the top and bottom side.

PCB C: Double Sided – Maximum Vias. This 4 layer board is the SP7655 standard evaluation board. It is similar to 'B' but has numerous vias throughout all of the main copper areas of Vin, Vout, Ground, and the inductor pads. This further increases the heat sinking capability of the PCB. The layout places components on the top and bottom side.



A

B

C

Figure 1

Methodology

Data was collected using derating equipment and methods common to the DC-DC converter module industry shown in Figures 3 and 4. Each board was mounted in the airflow chamber so that the airflow is across the PCB from Vin to GND. In the case of the single layer board where the inductor placement would interfere more with the airflow over the device, both directions were compared.

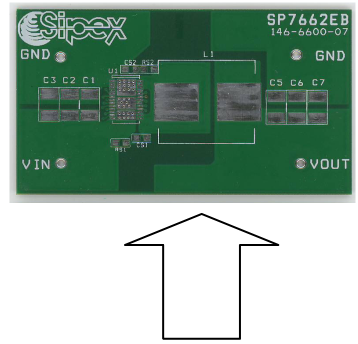


Figure 2

Temperature Controlled Airflow

Air temperature was regulated and airflow was laminar across the PCB surface. The PCB was also in the physical orientation shown here with air flowing from the floor to the ceiling and airflow, hitting the edge of the PCB across the device.

Temperatures were taken using a thermal imaging camera – FLIR Model A20, from FLIR Systems. Component temperature was recorded using the readout from the camera. Emmisivity was set for optimal temperature measurement of the PowerBlox^{TM} part. Due to the small thermal impedance between the device case and the device junction, the temperature displayed by the camera was recorded as the device junction temperature. Derating of the device was done by limiting the hottest spot on the PowerBlox^{TM} to 120˚C. At output power levels beyond ~5 Watts, the device MOSFETs would measure as the hottest areas – leaving the controller 10 or more degrees cooler than the FET. This provides further margin in the derating of the part as the controller junction is rated to 125˚C and the MOSFETs are junction-rated to 150˚C.

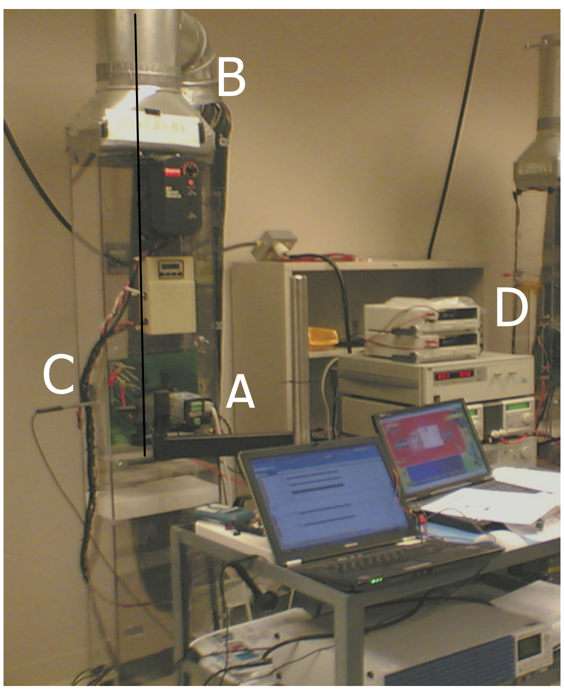


Figure 3 – Chamber Set-up

A - Thermal Camera
B - Laminar Airflow Chamber
C - Airflow Meter
D - Source and Loads
E - Device Under Test

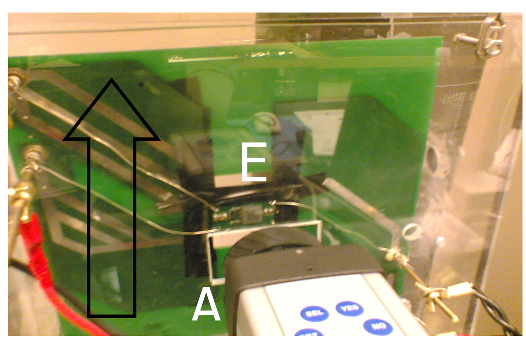


Figure 4
DUT and Infrared Camera – arrow showing airflow direction.
Eval board is mounted to a larger test fixture but is not soldered to the fixture. No additional heat sinking was added to the eval board.

Understanding the Thermal Images

A description of the temperature measurements and plots are shown in Figure 5 and 6.

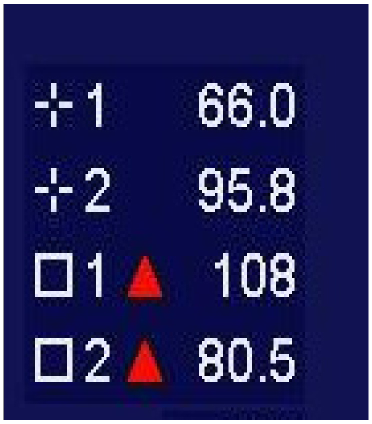


Figure 5

Camera Readings:

+1 - The temperature measured at the center of cursor cross hair 1

+2 - The temperature measured at the center of cursor cross hair 2 (Typically the low-side FET)

☐1∆ -The hottest temperature measured in BOX 1 (Typically the high-side FET)

☐2∆ - The hottest temperature measured in BOX 2 A cursor is not shown indicating the hottest spot as in Box 1 (This is the inductor core material temperature)

Sample Image:

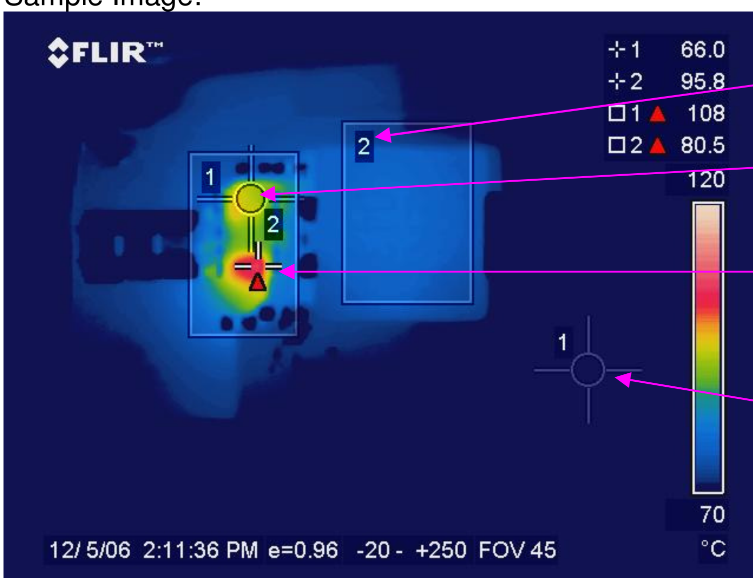
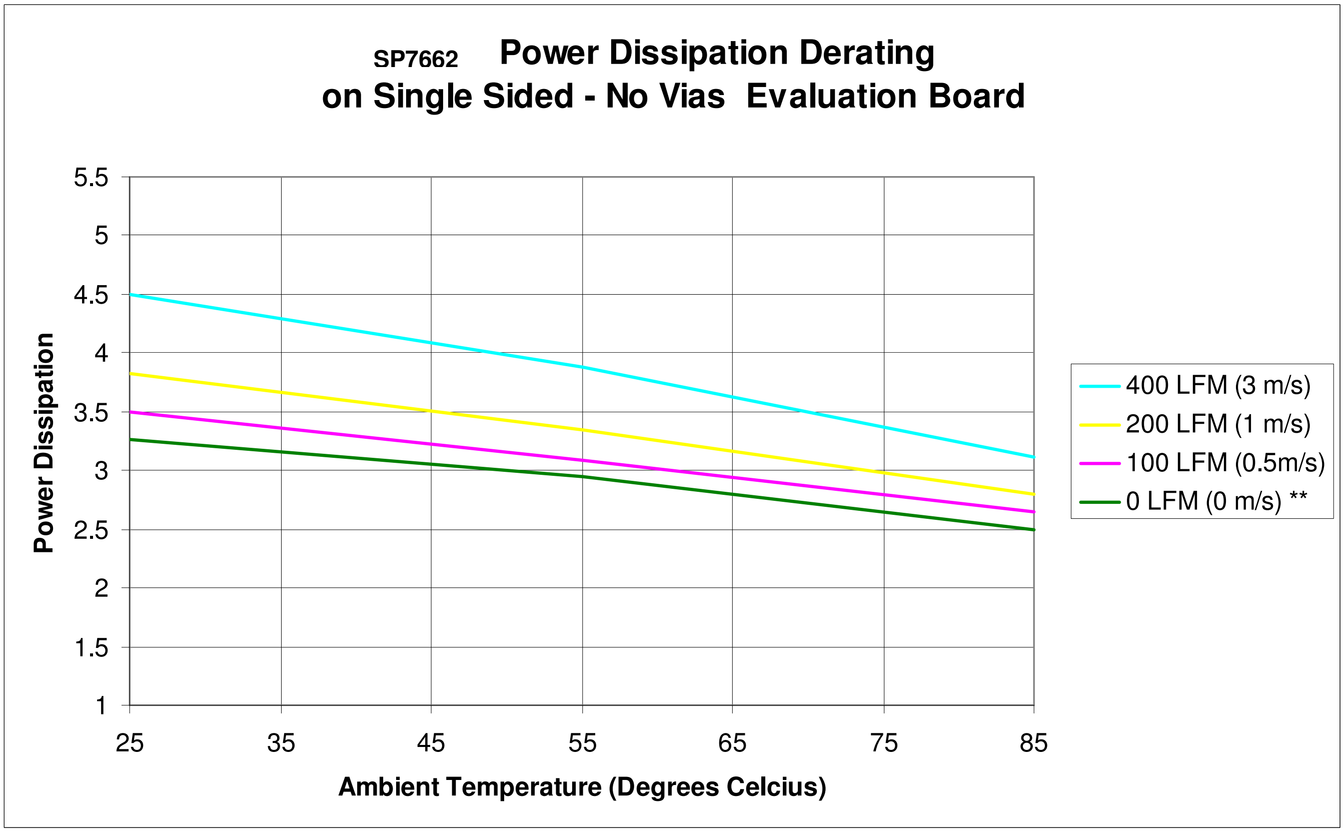
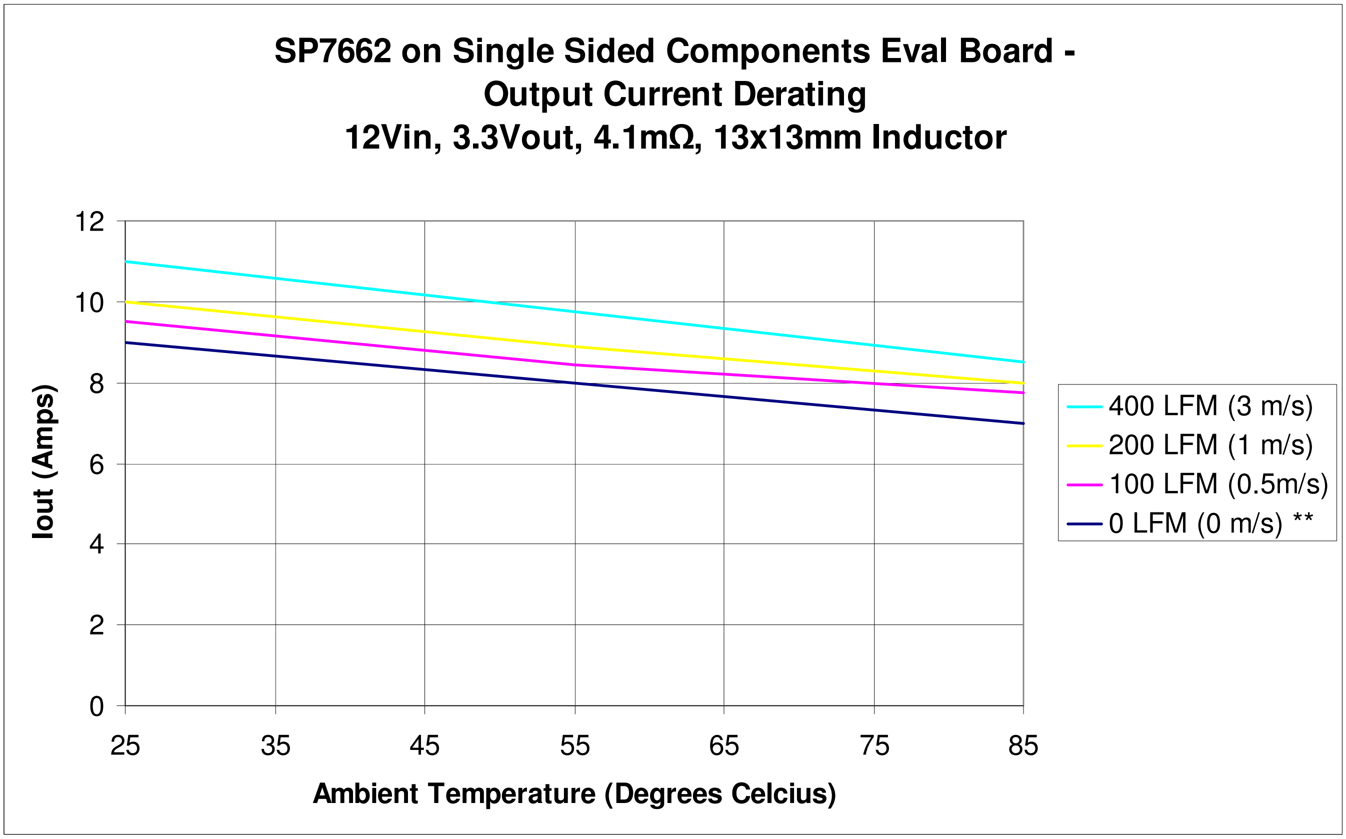


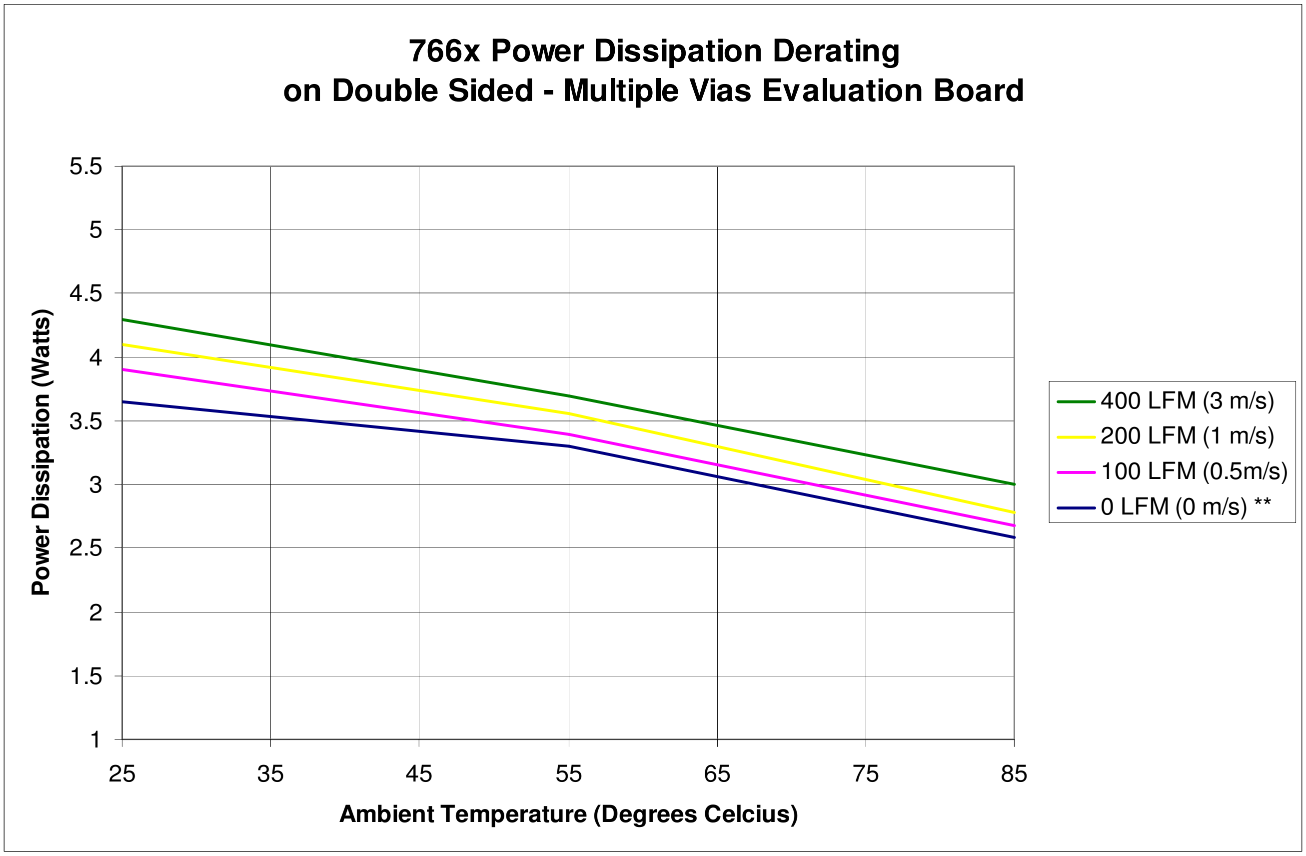
Figure 6

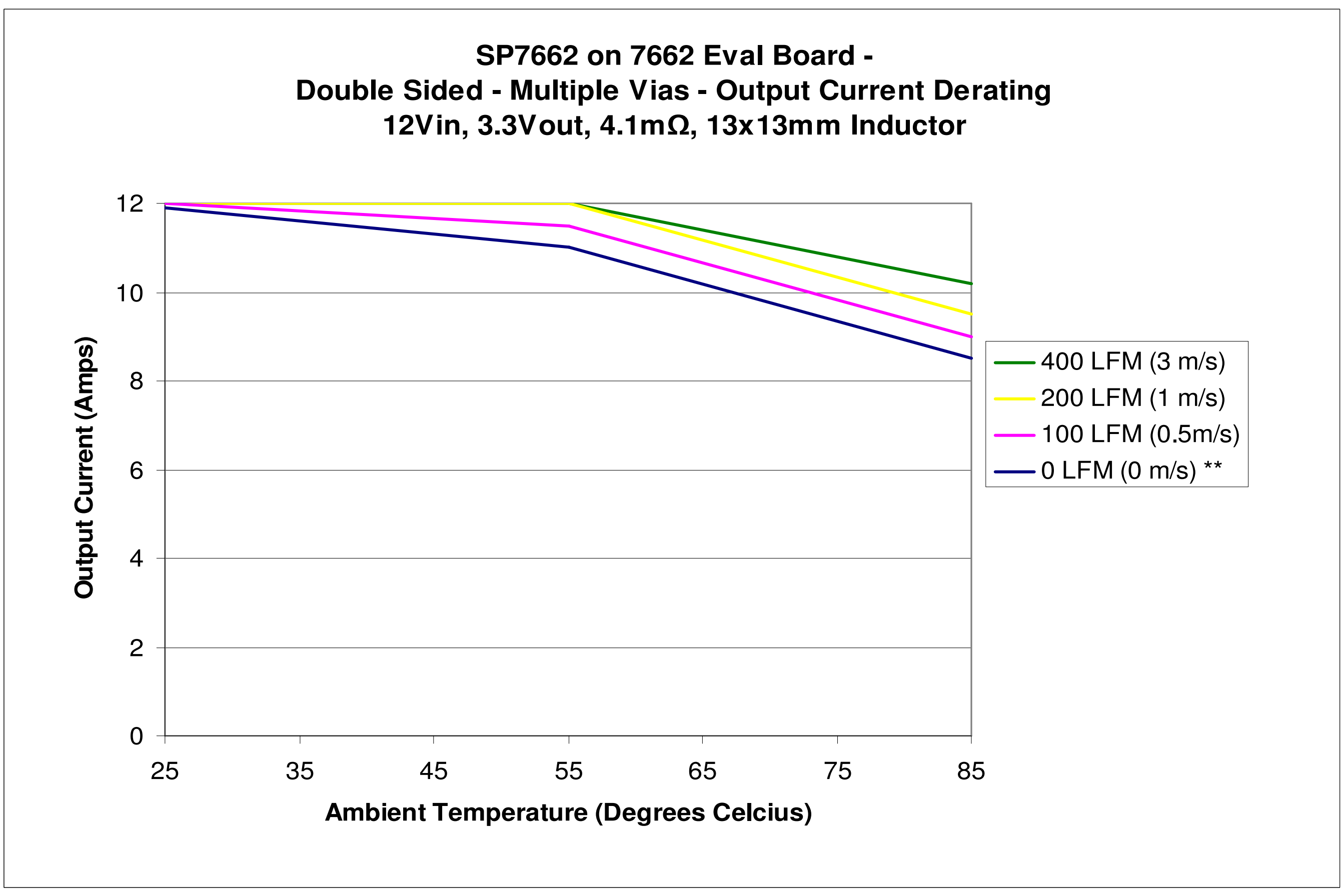
Results: PCB A – Single Sided Components – No Vias – Derating / SOA



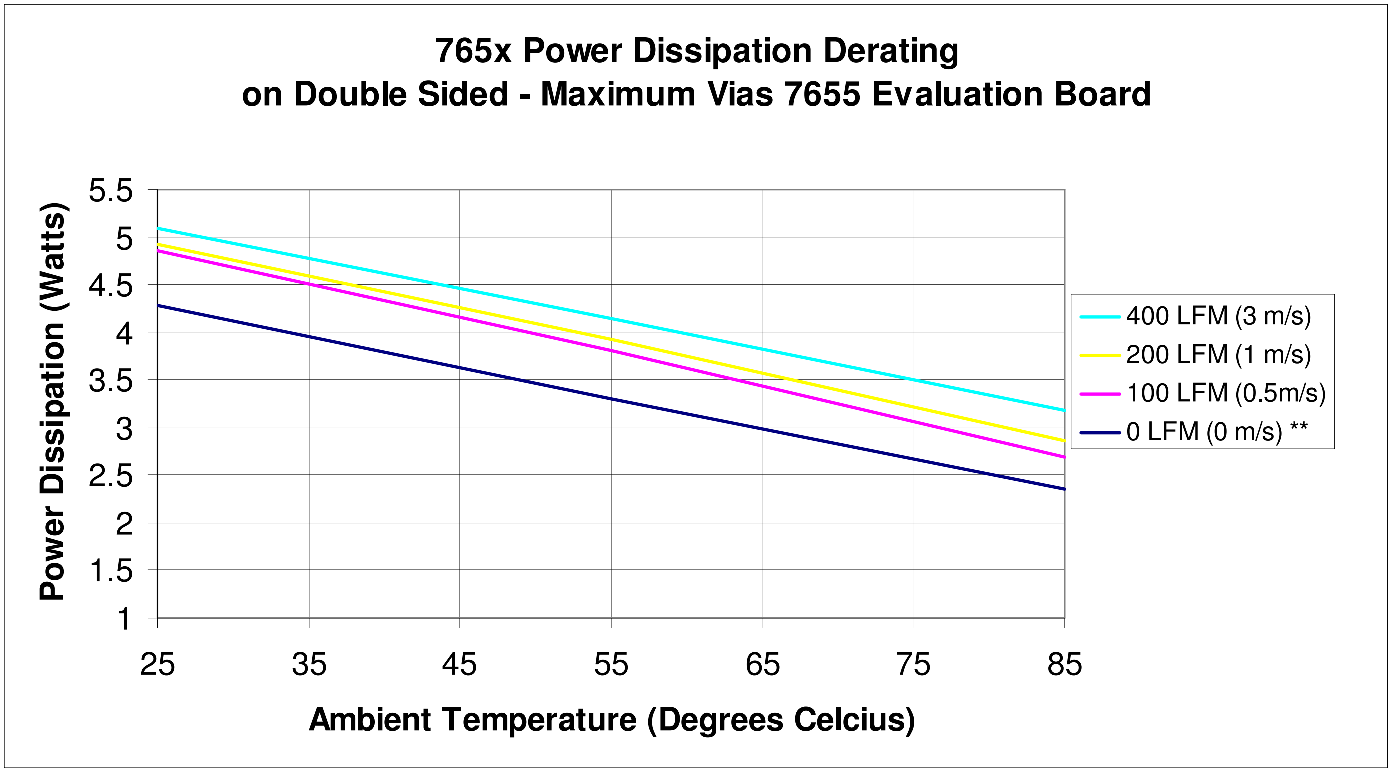


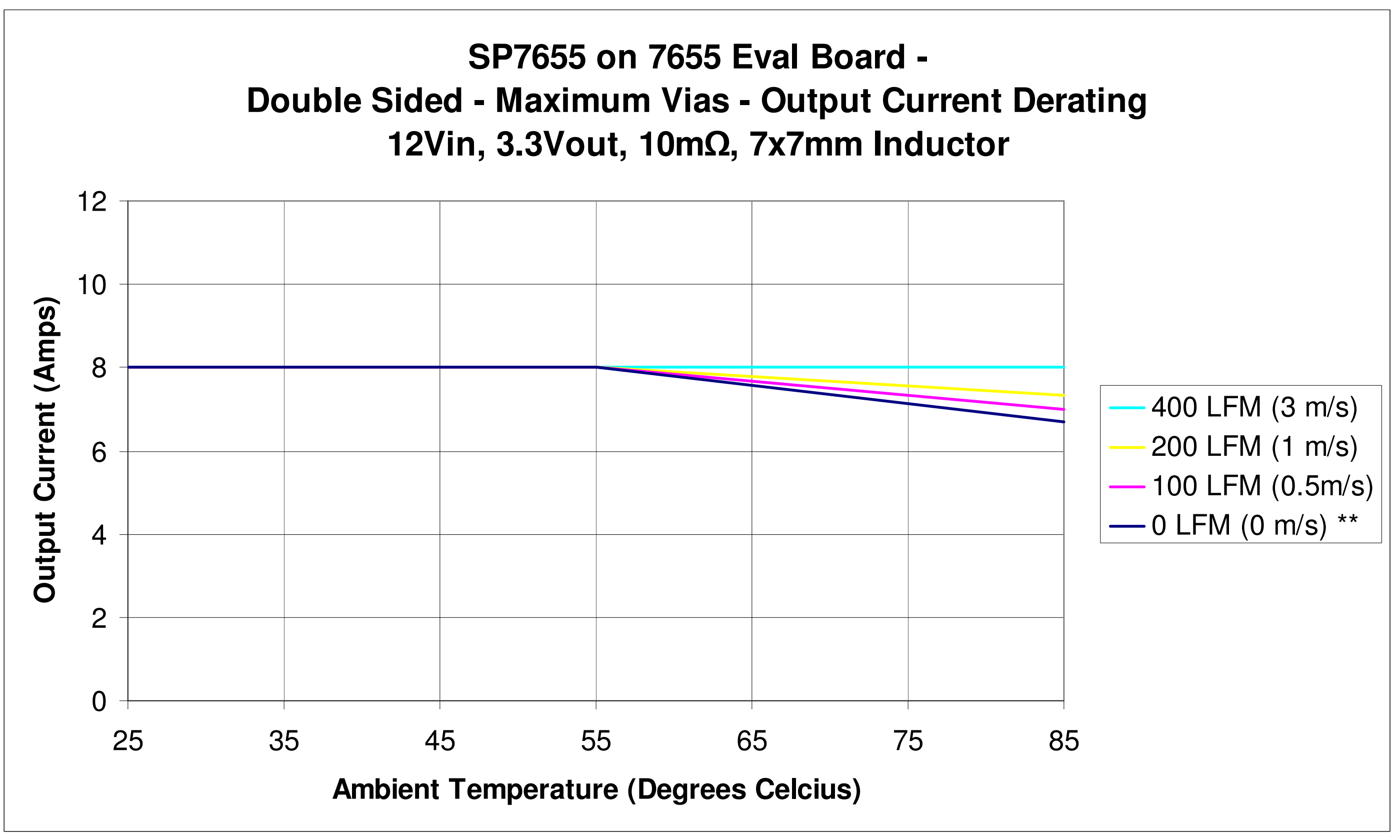
Results: PCB B - Double Sided Components – Multiple Vias PCB – Derating / SOA





Results: PCB C - Double Sided Components - Maximum Vias – Derating / SOA





Note: 7655 Maximum Output Current is 8Amps

Power Dissipation vs. Temperature Results Analysis

In general the achievable power dissipation for all PCBs, SP7662, and SP7655 devices was similar. The highest achievable power dissipation was measured on the SP7655 PCB with maximum vias and 400lfm (linear feet per minute) of airflow at 25˚C at approximately 5Watts. The following chart summarizes the results:

Power Dissipation (Watts)	0lfm	400lfm
25 Degrees		
PCB A– Single Sided 766x – No Vias	3.3	4.5
PCB B– Double Side 7662 – Multiple Vias	3.7	4.3
PCB C– 7655 Eval Board – Maximum Vias	4.3	5.1
85 Degrees		
PCB A– Single Sided 766x – No Vias	2.5	3.1
PCB B– Double Side 7662 – Multiple Vias	2.6	3
PCB C– 7655 Eval Board – Maximum Vias	2.4	3.2

* lfm – linear feet per minute

All three boards at 0 lfm and 85˚C are generally similar, we can basically call them the same. This was also true at 85˚C and 400lfm. A larger difference shows up at 25˚C and 0 lfm where there is a greater delta between the component surfaces and the air temperature. Under this condition, any paths for heat transfer are fully utilized and the effects of more copper attached to the device can be seen. When 400lfm of airflow is added, the A and B boards perform similarly, and again the board with more vias has the greater cooling ability. Also in PCB A the PowerBlox™ is in a rotated orientation and has a more open layout compared to the other boards. Airflow across the device is less restricted and would account for the slightly better performance at 400lfm than PCB B.

The straight current derating of each supply is summarized below and can be used for the individual supplies and as a guideline.

Maximum Output, 12Vin, 3.3Vout	0lfm	400lfm
25 Degrees		
PCB A– Single Sided 766x – No Vias	9	11
PCB B– Double Side 7662 – Multiple Vias	12	12
PCB C– 7655 Eval Board – Maximum Vias	8 (max limit)	8 (max limit)
85 Degrees		
PCB A– Single Sided 766x – No Vias	7	8.5
PCB B– Double Side 7662 – Multiple Vias	8.5	10
PCB C– 7655 Eval Board – Maximum Vias	6.7	8

Note that each supply will have a different efficiency for a given output current, and hence a difference power dissipation. Also, the SP7655 supply used a smaller 7x7mm inductor which gives it a disadvantage compared to the other eval boards. The smaller package and higher DCR caused the part to generate significantly more heat. As will be shown in the thermal images of the SP7655 supply, the inductor runs very hot compared to the 13x13mm inductors and makes the performance worse by heating the SP7655 part.

Results Comparison

A ‘Power Dissipation Derating Curve’ was generated for each system to act as a guideline for various PowerBlox™ solutions operating in various conditions. The versatility of the PowerBlox™ parts in end applications makes a more general approach to its characterization necessary. The following is an example comparing the tested results.

Using the SP7662 Standard Evaluation Board - PCB B – and the same derating fixture and set-up - a 20Vin, 1.8Vout supply was tested. The power dissipation figures are checked against our new data on a few points. The supply used a 13x13mm, 3.5mΩ inductor, but of a lower profile than the previous 3 test examples. The 9% duty ratio versus the previous 27.5% duty ratio, and the higher Vin which will demand more of the internal LDO, introduces a very different operating condition for the supply.

* Note that in all calculations of PowerBlox™ power dissipation the power dissipation of the inductor DCR is subtracted from the overall power dissipation of the converter to obtain the power dissipation of the PowerBlox™.

Example:
Condition 1: 0 lfm, 25 degrees, SP7662 on 7662 multiple vias eval board (PCB B)
Condition 2: 100lfm, 85 degrees, SP7662 on 7662 multiple vias eval board (PCB B)

	Vin (volts)	Vout (volts)	Efficiency	**Power Blox Pdiss**	**Quoted Pdiss Limit for 120˚C Case Max**	**Peak Case Temperature Measurement**
Condition 1	20	1.8	83.44%	**2.82 Watts**	**3.7 Watts**	**86.5˚C**
Condition 2	20	1.8	82.89%	**2.00 Watts**	**2.68 Watts**	**100˚C**

When less than recommended power was dissipated in the device, we can see the temperature of the device was lower than 120˚C.

Unfortunately the requirements for this test were a maximum case temperature of 100˚C so we can not test the full 120˚C limit of our results, however it still shows the figures are good. In condition 2 the supply is dissipating 0.68Watts less power than the recommended maximum and it is 20 degrees cooler.

Summary

The versatility of the PowerBlox™ family means that power supplies can be created with a very large number of variations in Input Voltage, Output Voltage, Output Inductor value and package size, as well as Layout. All of these factors influence the thermal performance of the device. To use an Output-Current-only Derating curve and apply it to any PowerBlox™ solution would be entirely reckless. The Output Current derating curves should be used as a performance guideline for the solutions presented. The Output Power Dissipation Derating is a much better way to predict the thermal performance of any solution.

Derating of devices was done by limiting the hottest spot on the PowerBlox™ to 120˚C. In the case of the SP7662 devices, this spot was always associated with the high side FET. In the case of the SP7655, this spot was always the low side FET. In both cases the controller (the center of the device) was 10 or more degrees cooler then the FET. This provides further margin in the derating of the part as the controller junction is rated to 125˚C and the MOSFETs are junction-rated to 150˚C

Results:

Power Dissipation (Watts)	**0lfm**	**400lfm**
25 Degrees		
PCB A – Single Sided 7662	3.3	4.5
PCB B – Double Side 7662	3.7	4.3
PCB C – 7655 Eval Board w/multiple vias	4.3	5.1

This data can be used to predict a safe operating region for various PowerBlox™ power supplies operating on a variety of PCBs under a variety of input, output, inductor choices, and resulting efficiencies.

For more information on the thermal resistance of the PowerBlox™ you can refer to the application note ANP5 'Thermal Resistance on 765x Devices ' from this link: http://www.sipex.com/applicationNotes.aspx?p=appNotesPower . ANP5 characterizes the PowerBlox™ device on various PCB layouts as a singular device. Keep in mind the results in ANP5 do not include thermal effects of the presence of the output inductor.

APPENDIX

Thermal Scans

Airflow is always from the bottom to top of the image
Note: The thermal camera automatically adjusts the scale, colors and temperature minimums and maximums are not always the same.

Layout Plots

Layout Design Tip: Copper areas under the Power Blox and Inductor are important and help with device power dissipation even when not electrically connected by vias.

Results: PCB A – Single Sided, No Vias, 4 Layer PCB

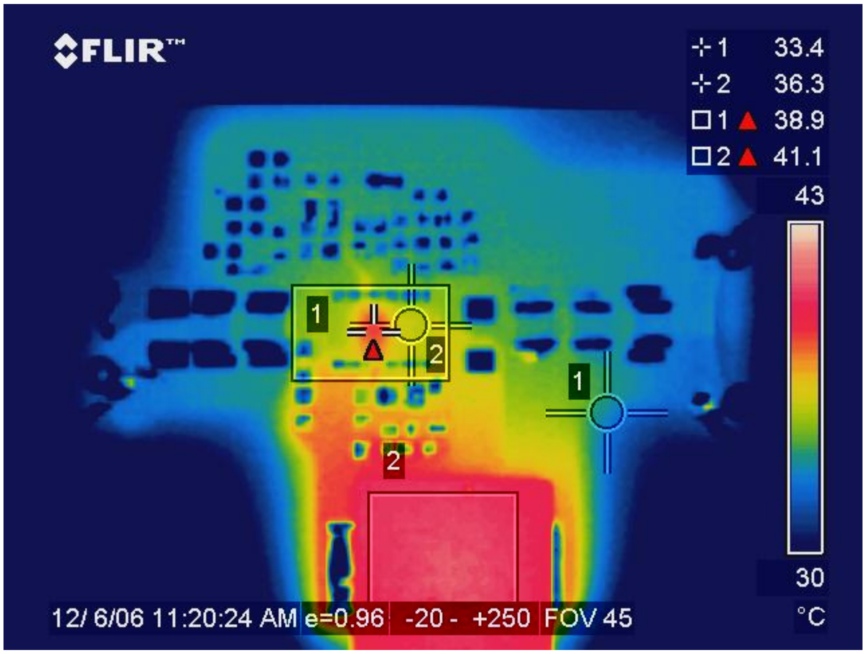


Image 1 – Vin: 12V Iout: 0Amps Ambient Temp: 25˚C Airflow: 0lfm Pdiss: Minimum

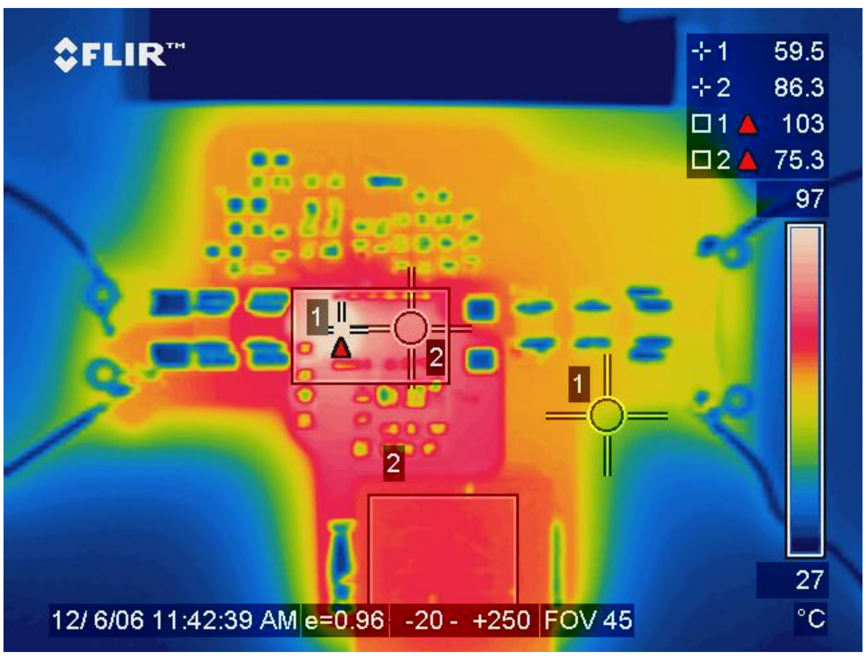


Image 2 – Vin: 12V Iout: 8.0Amps Ambient Temp: 25˚C Airflow: 0lfm Pdiss: 3.1W

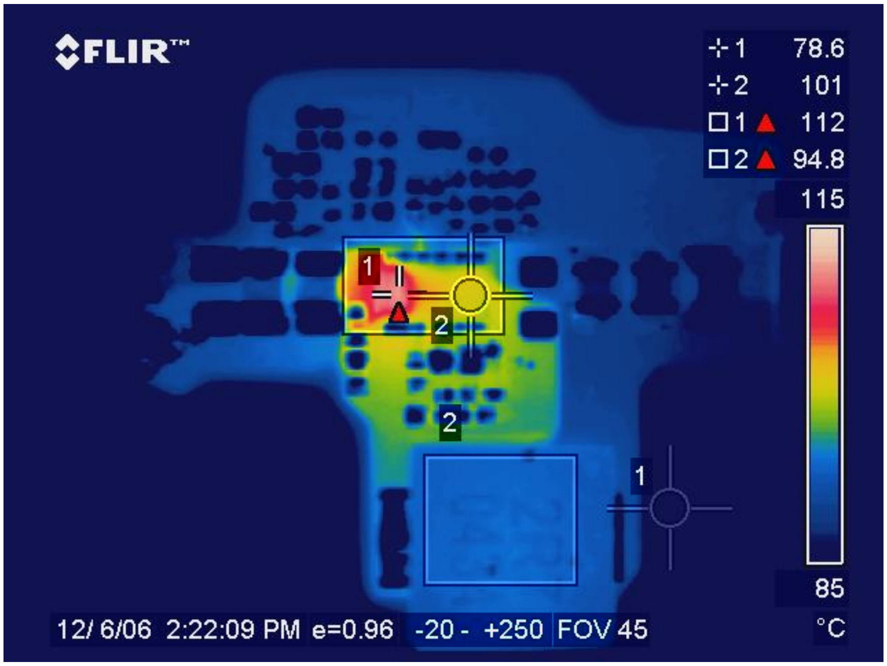


Image 3 – Vin: 12V Iout: 6.75Amps Ambient Temp: 85˚C Airflow: 400lfm Pdiss: 2.48W Orientation #1

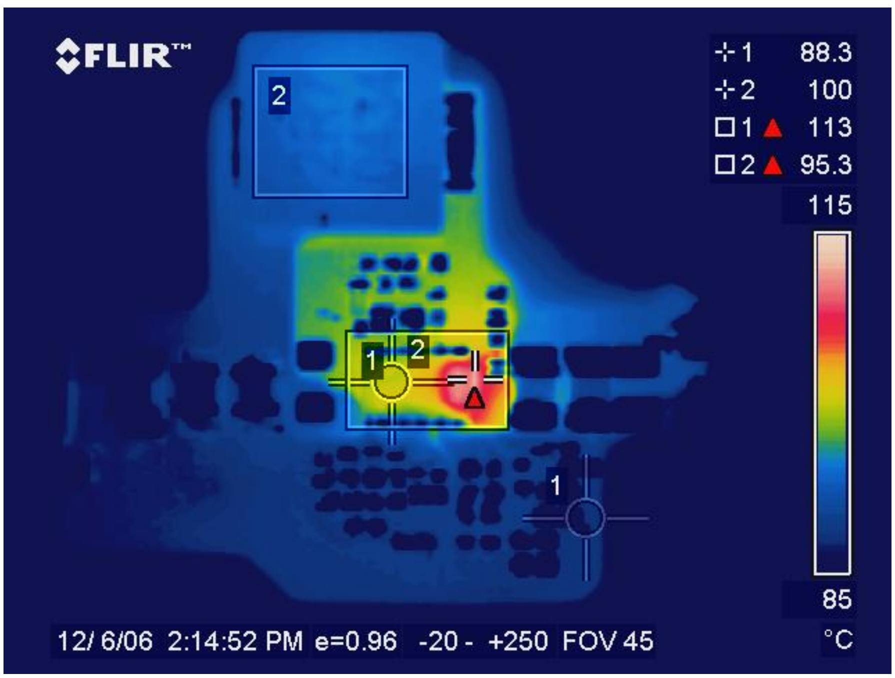


Image 4 – Vin: 12V Iout: 6.75Amps Ambient Temp: 85˚C Airflow: 400lfm Pdiss: 2.48W Orientation #2

Almost no difference is seen in temperature for this example.

Results: PCB B – Double Sided, Multiple Vias, 4 Layer 7662 Evaluation PCB

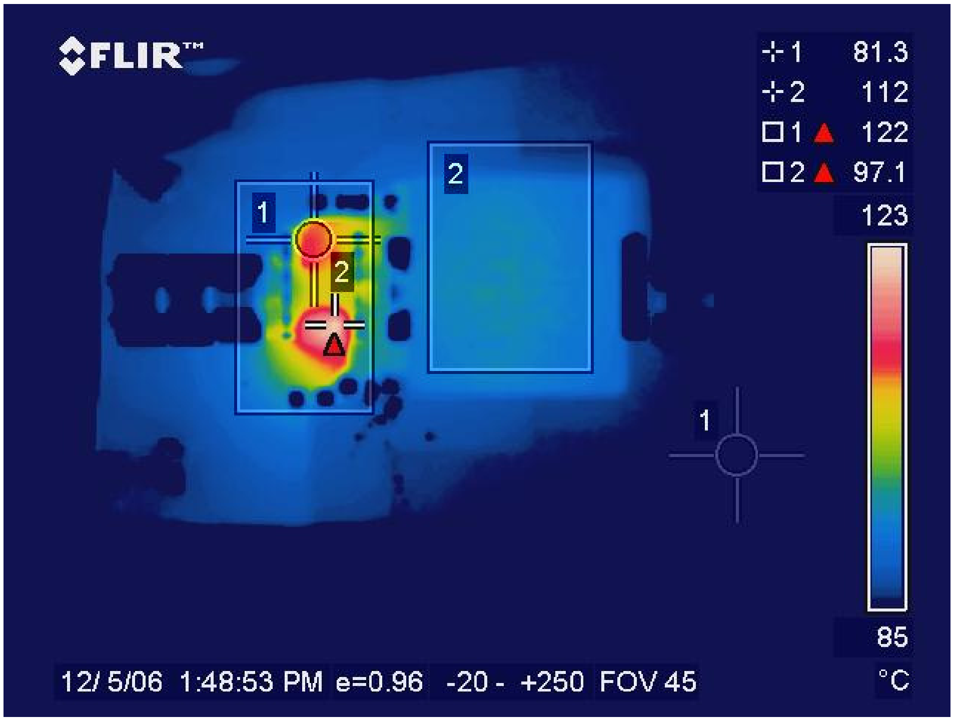


Image 5 – Vin: 12V Iout: 12Amps Ambient Temp: 25˚C Airflow: 0lfm Pdiss: 3.65W

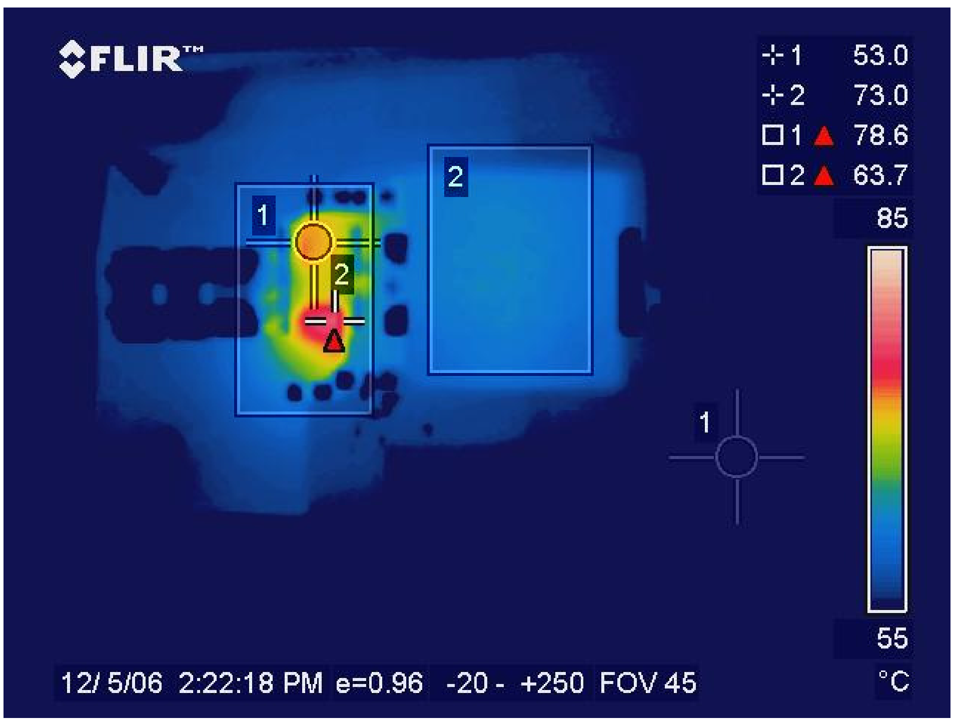


Image 6 – Vin: 12V Iout: 10Amps Ambient Temp: 25˚C Airflow: 100lfm Pdiss: 2.84W

Results: PCB C – Double Sided, 4 Layer, Maximum vias 7655 Evaluation PCB

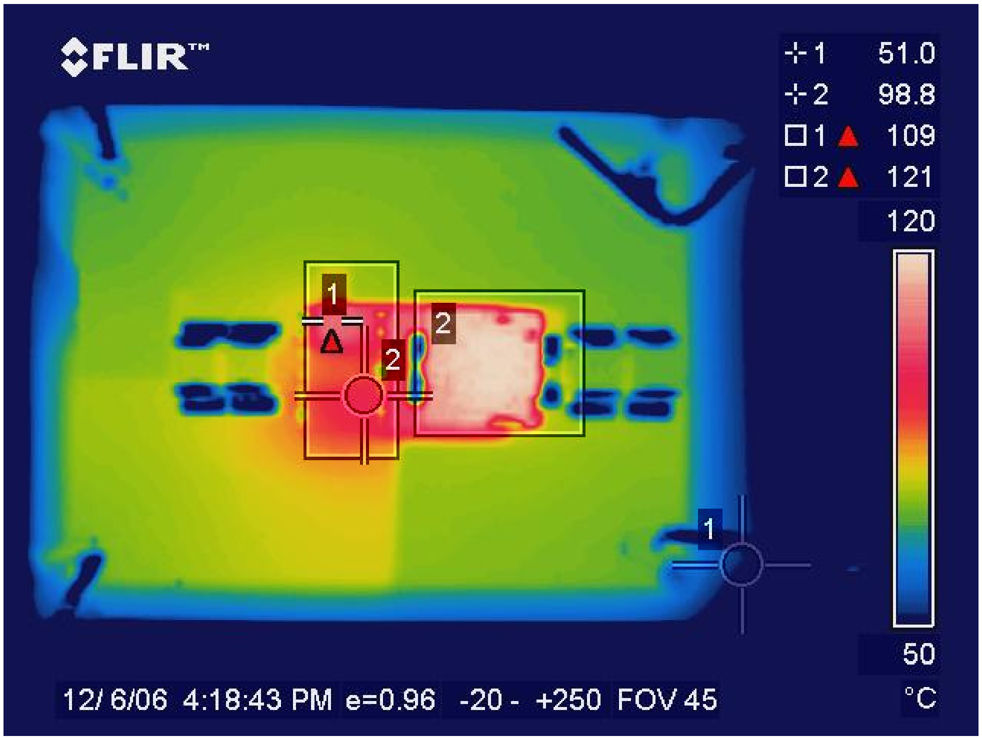


Image 7 – Vin: 12V Iout: 8Amps Ambient Temp: 25˚C Airflow: 0lfm Pdiss: 3.73W

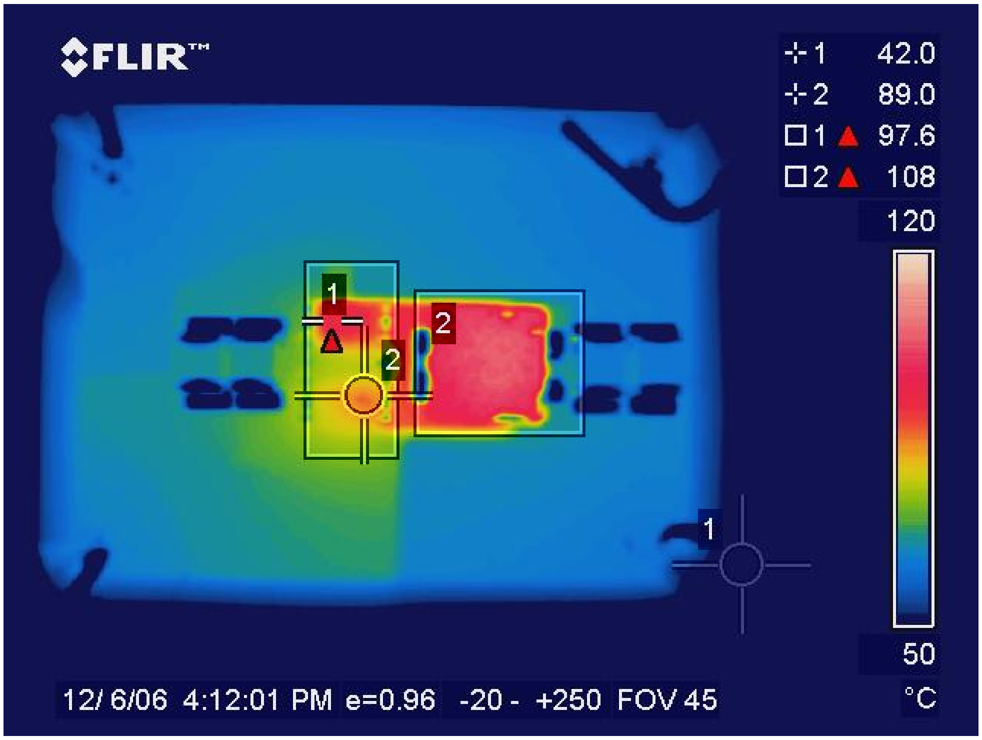
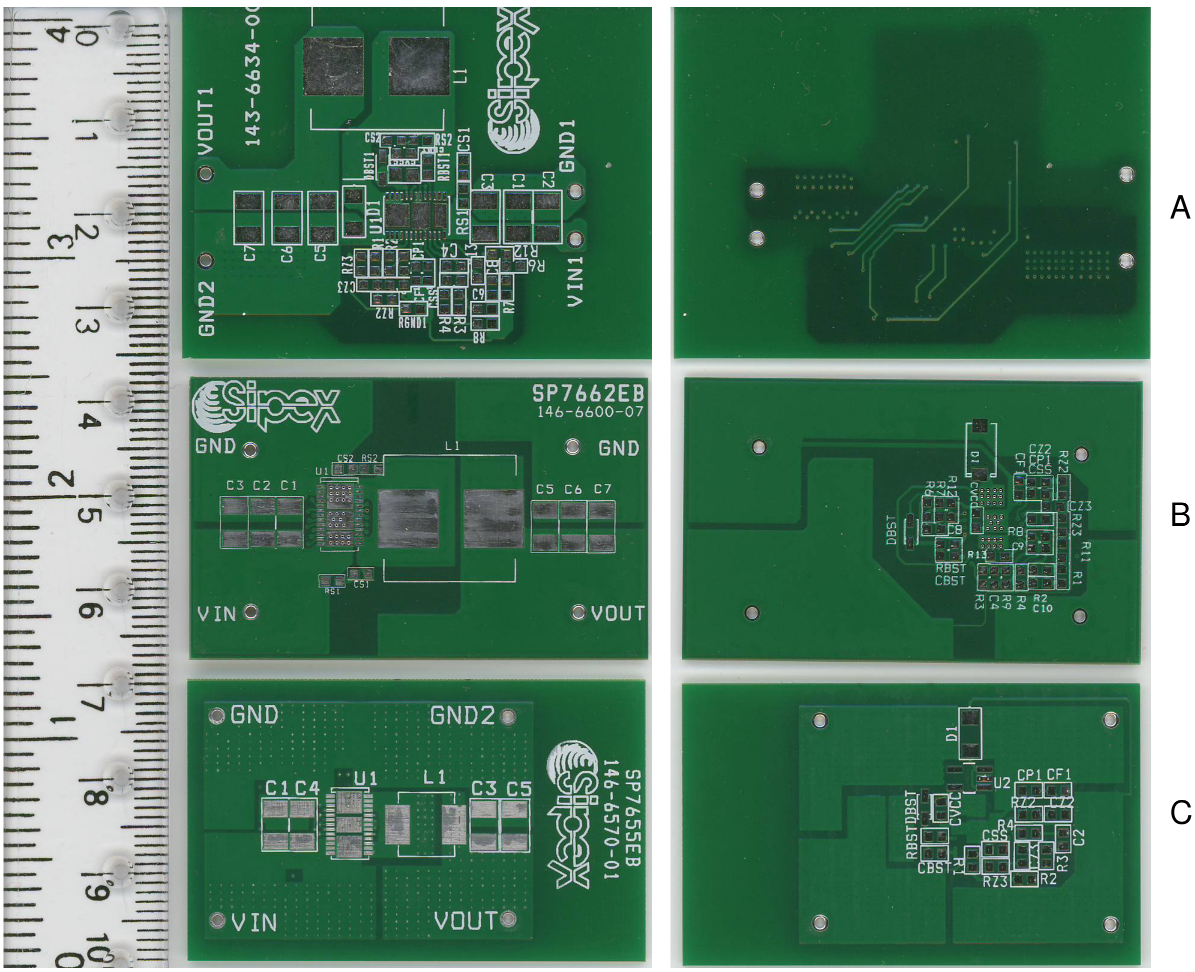


Image 8 – Vin: 12V Iout: 8Amps Ambient Temp: 25˚C Airflow: 100lfm Pdiss: 3.8W

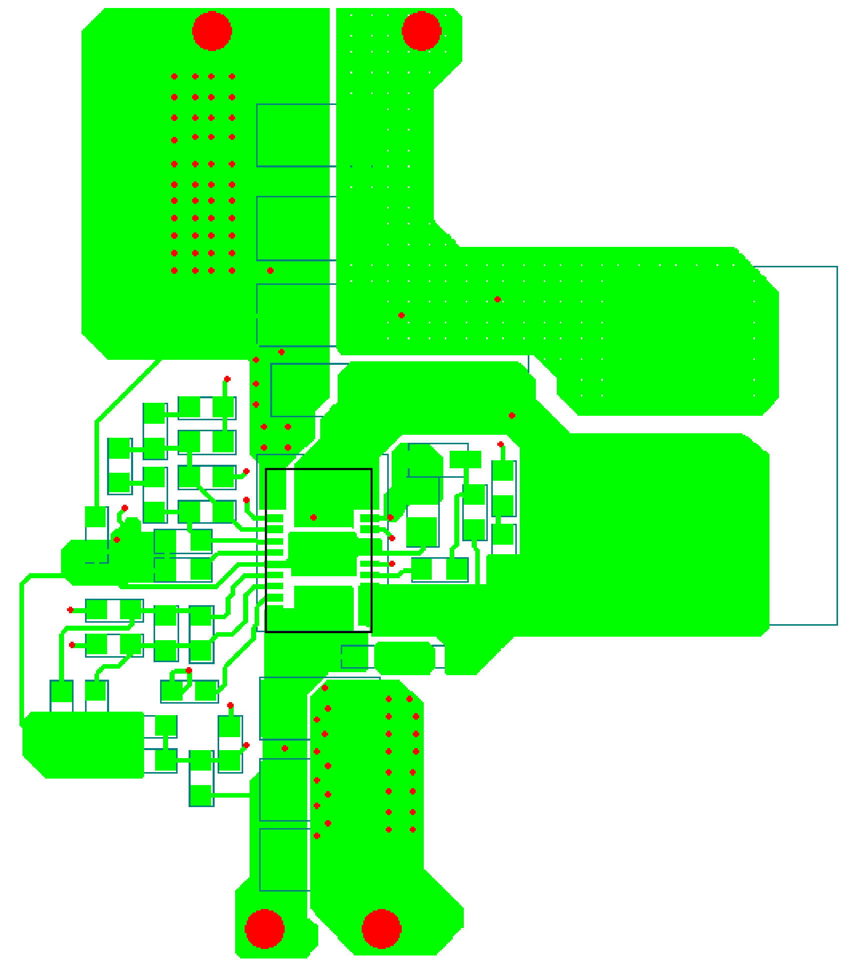
PCB Plots

PCB Image Comparison

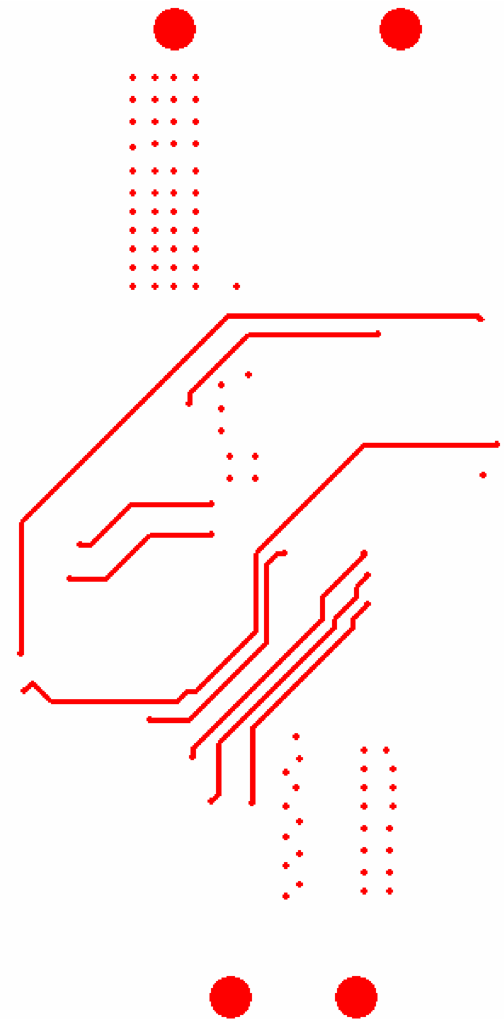
Top Side **Bottom Side**



PCB A – Single Sided Components PCB – 4 Layers

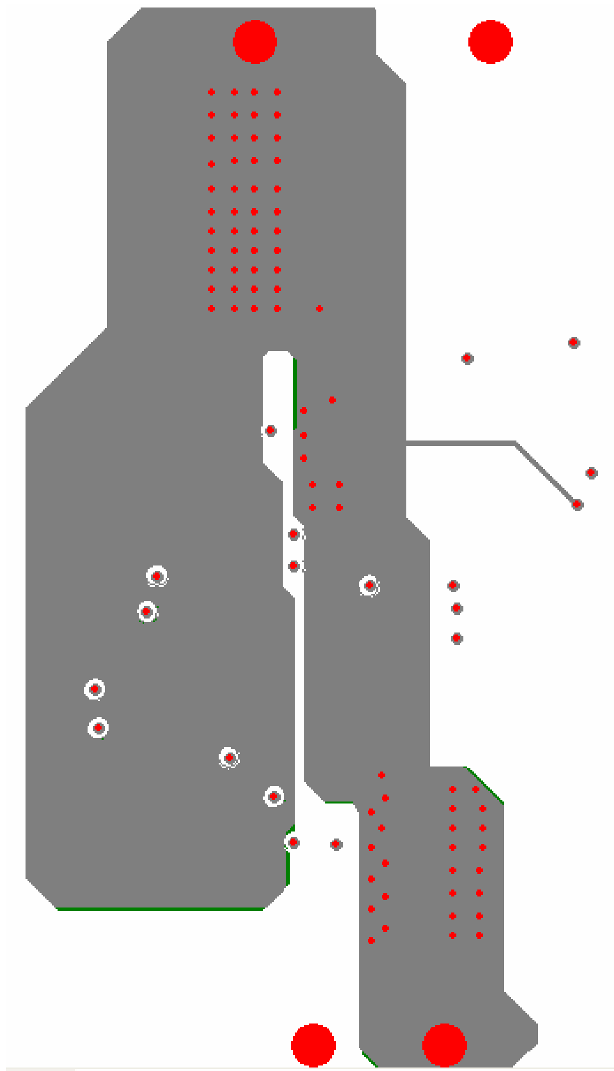


Top side traces and copper areas. Red circles are board vias

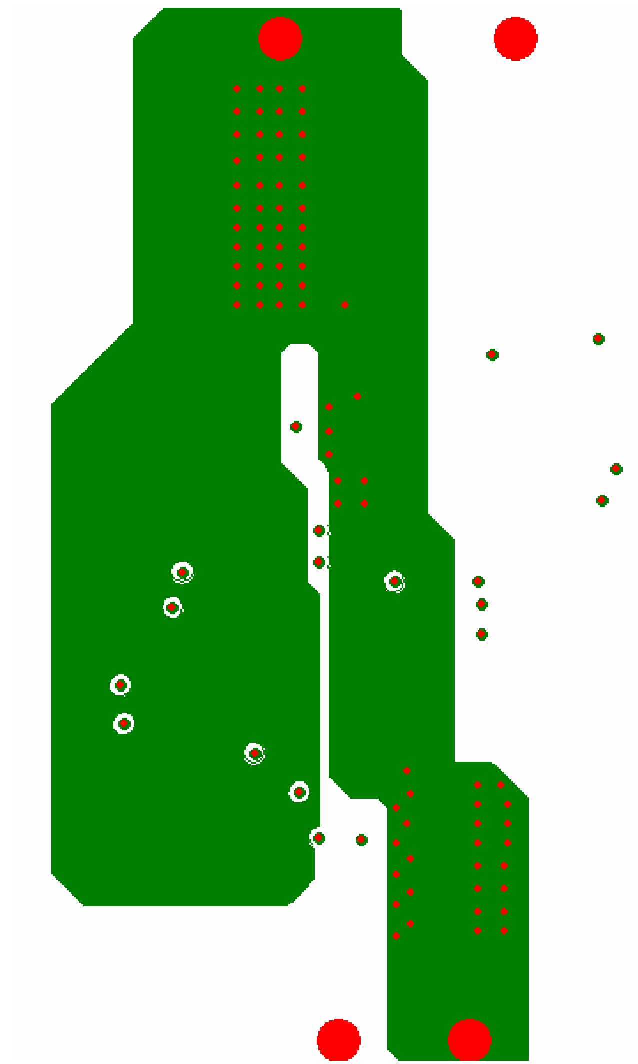


Back side

PCB A – Single Sided Components PCB – 4 Layers

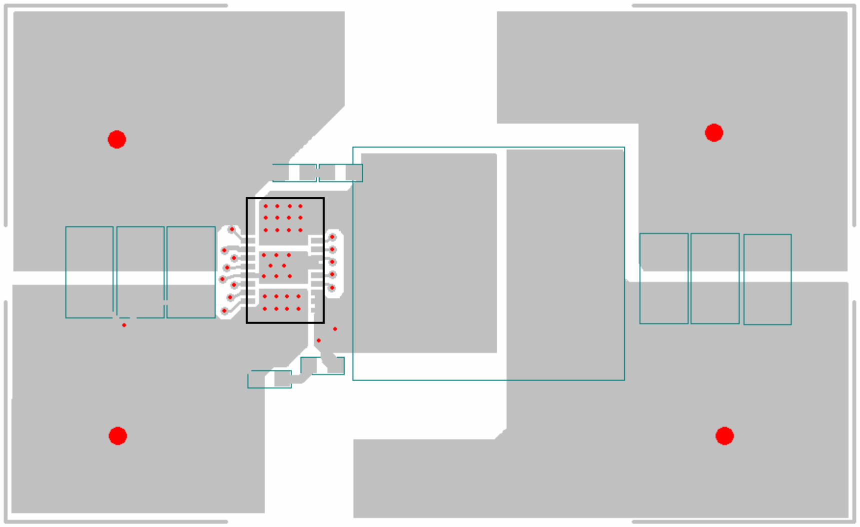


Internal Layer 2

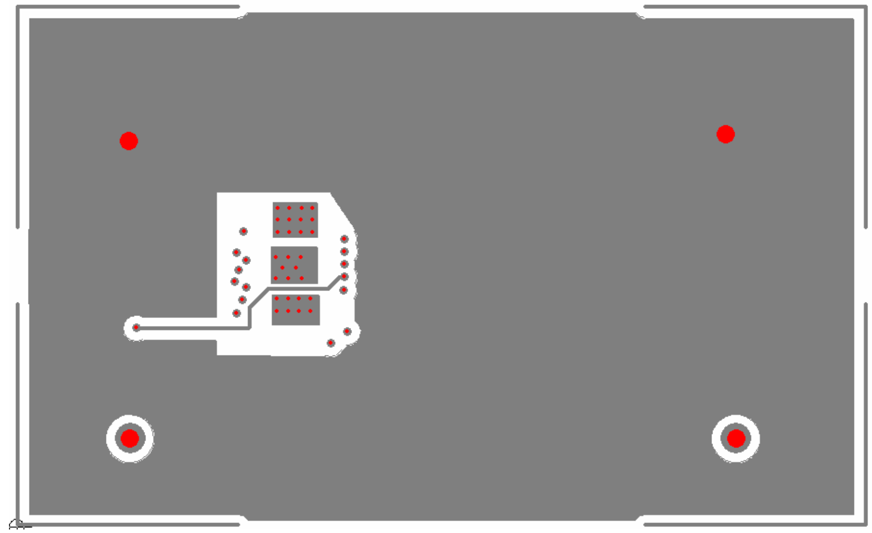


Internal Layer 3

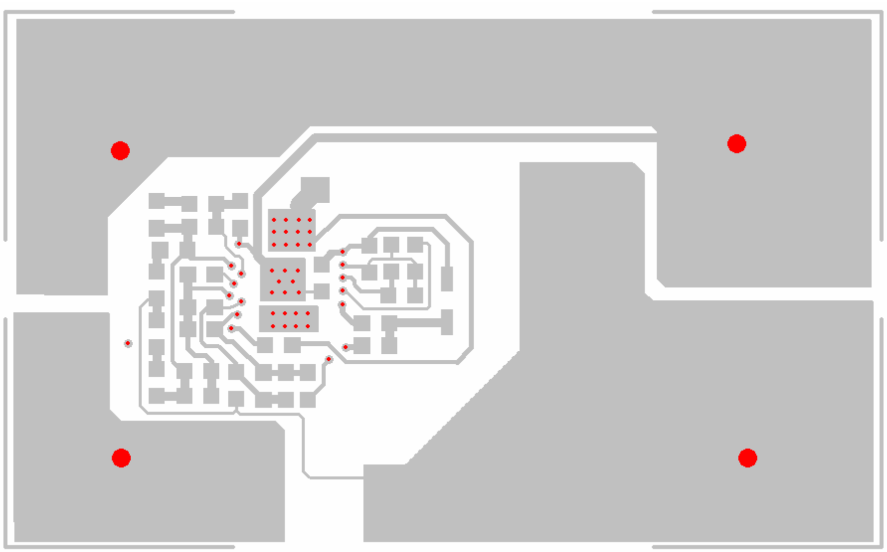
PCB B – Double Sided Components PCB – 4 Layers



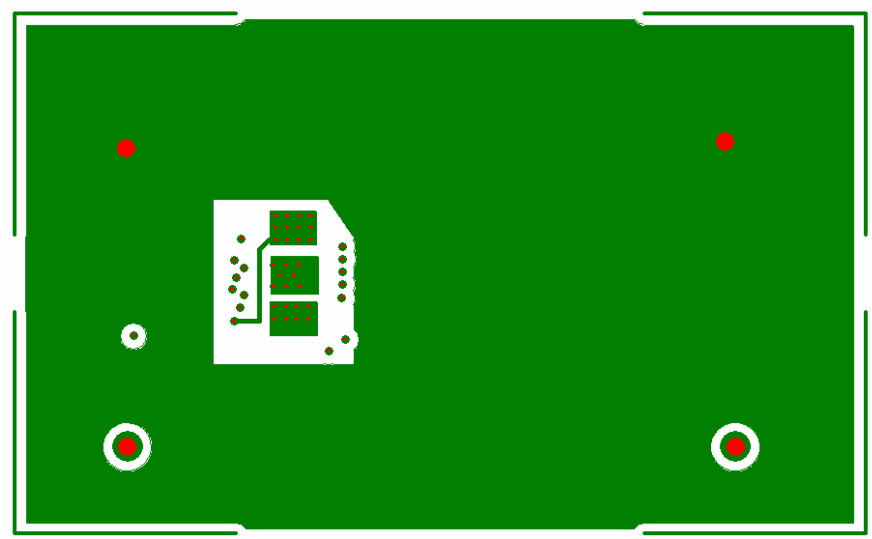
Top Layer



Inner Layer 2

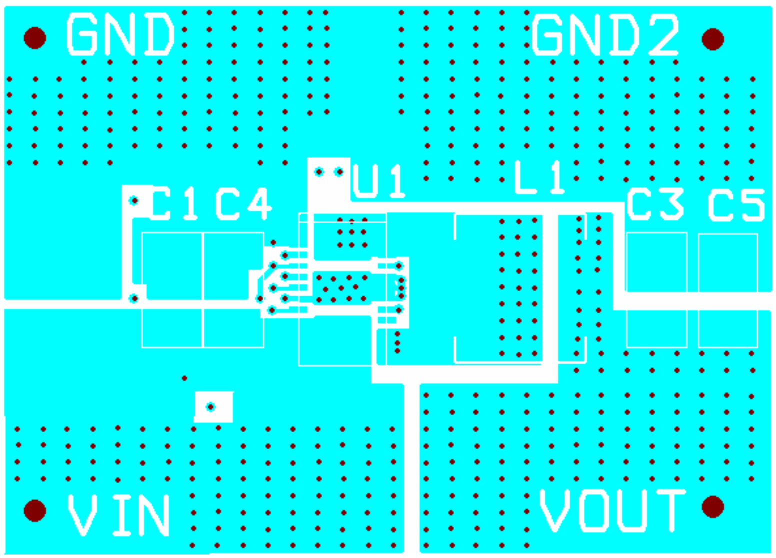


Bottom Layer

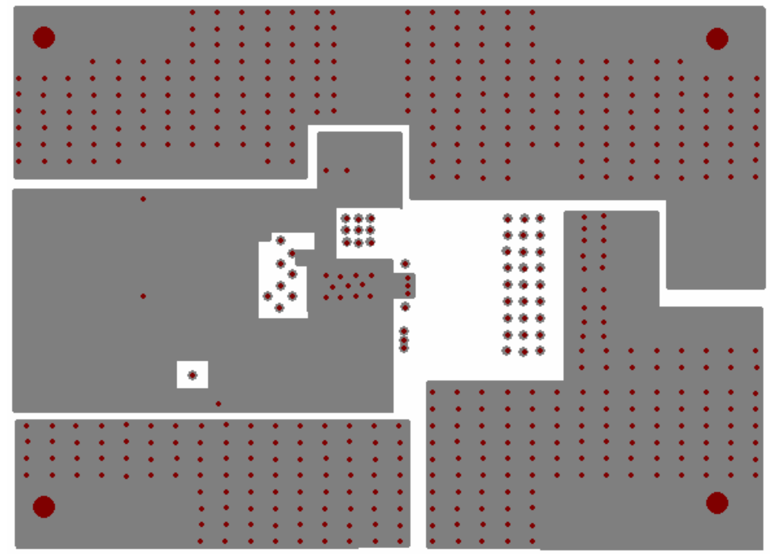


Inner Layer 3

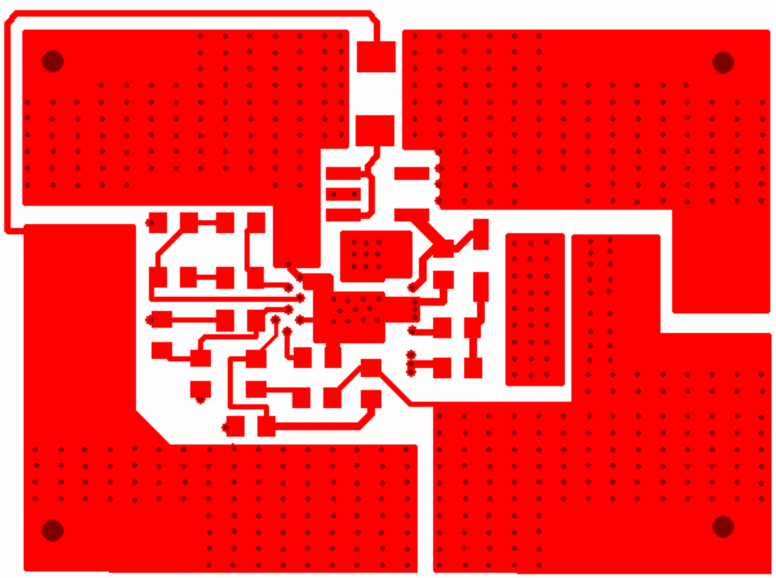
PCB C – Double Sided Components PCB – 4 Layers w/ Multiple Vias – 7655 Evaluation Board



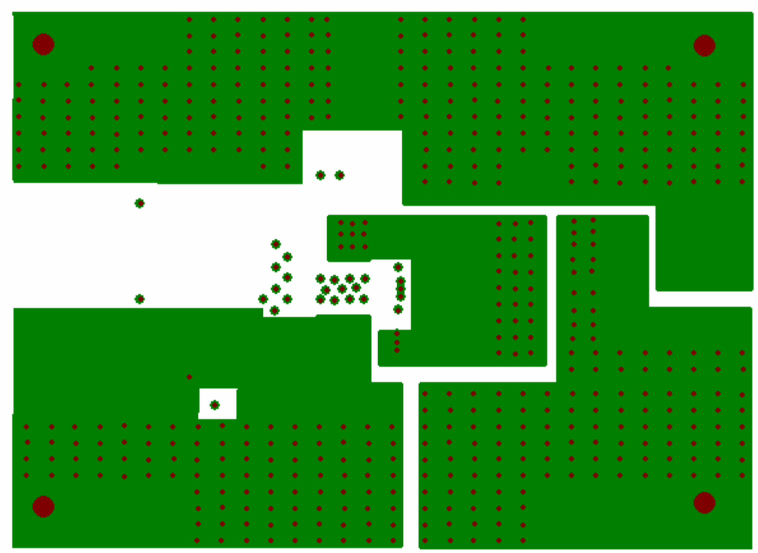
Top Layer



Inner Layer 2



Bottom Layer



Inner Layer 3