GENERAL DESCRIPTION

In some applications it would be more desirable to download a runtime image from a micro controller onto RAM than to store a configuration into flash memory. This document covers details on how to generate a runtime Intel HEX file, structure of the file, and procedure how to download the file from a micro controller to RAM.

This document applies to the following devices:

- XRP7724/7725
- XRP9710/9711

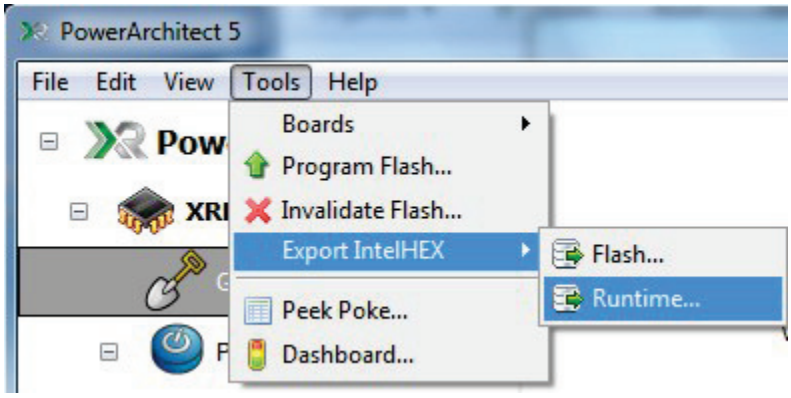
FEATURES

- **Overview**
- **Generating Runtime Intel HEX File**
- **Runtime Intel HEX File Overview**
- **Downloading Procedure**

GENERATING RUNTIME INTEL HEX FILE

The runtime image is generated using PowerArchitect™ design tool version 5 (PA5). NOTE: The functionality described here is only supported in PowerArchitect™ 5.02-r0 and later.

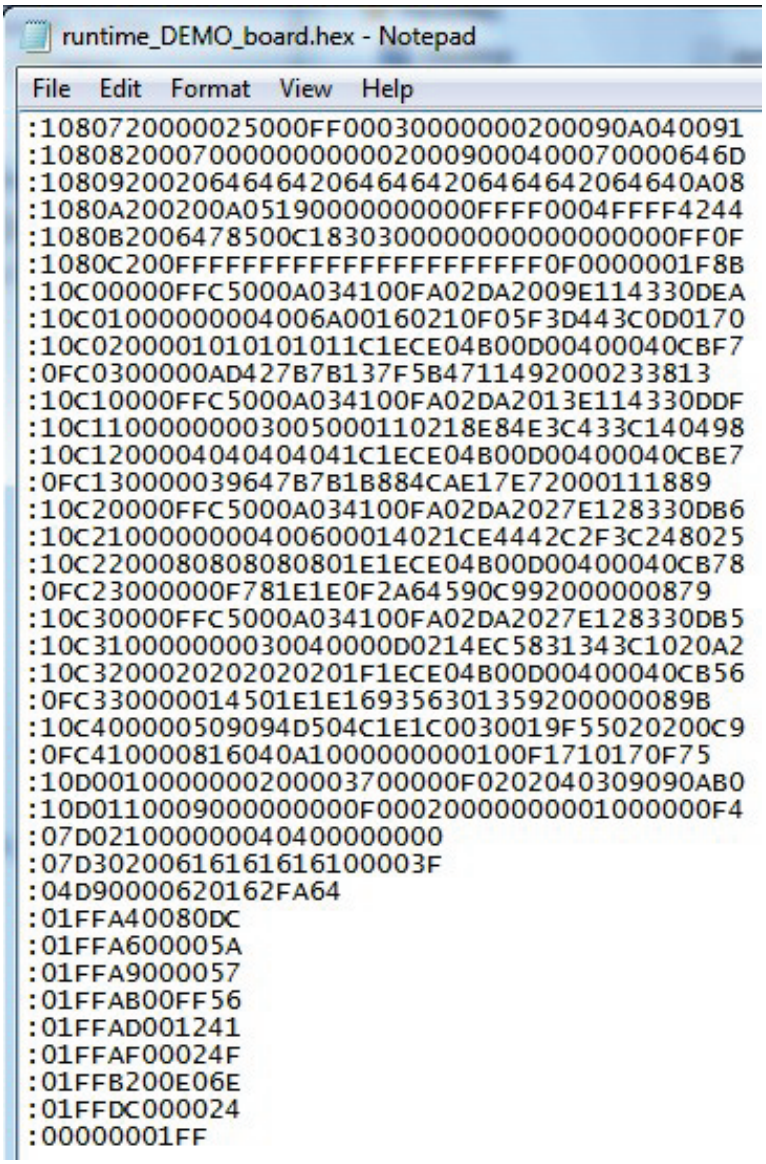
Once a design is complete in PA5, go to Tools, Export IntelHEX, and select Runtime…



Save the runtime HEX file.

RUNTIME INTEL HEX FILE OVERVIEW

Example of a runtime Intel HEX file is shown below.



The runtime image generated by PA5 follows the standard Intel HEX format described here:

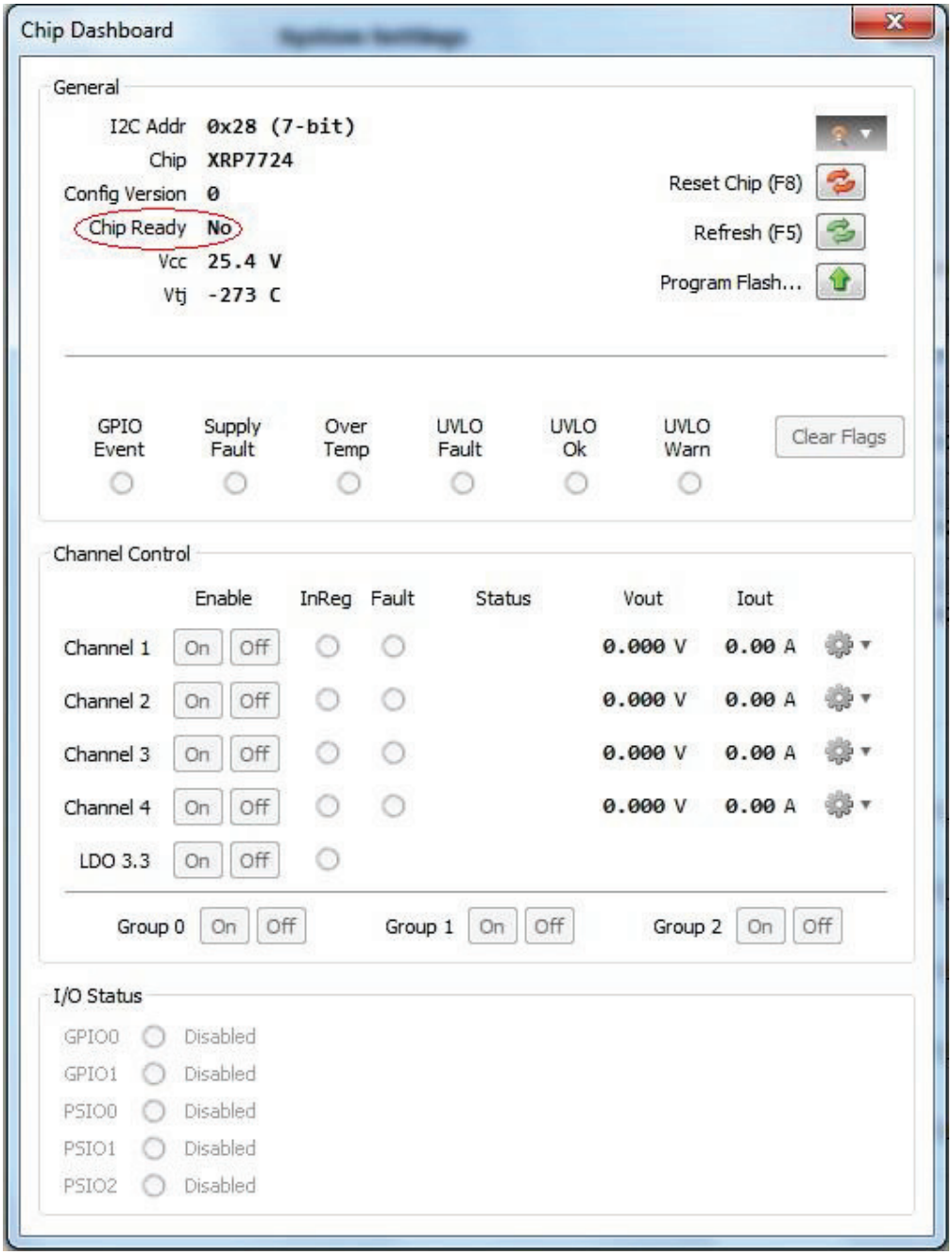
http://en.wikipedia.org/wiki/Intel_HEX

Note in the file above the address space is not continuous.

DOWNLOADING PROCEDURE

For the runtime image to be properly downloaded onto RAM two conditions must be met before the downloading process shall begin.

1. *There must be no valid configuration in flash memory that would be loaded into RAM at reset.* To check if this condition is met open the chip dashboard tool in PA5 and observe the Chip Ready setting. It ought to say No.



Similarly, the chip ready status can be verified via the I^2C command **PWR_CHIP_READY** (0x0E) (refer to ANP-38).

2. *The device must be reset before downloading process can begin.* This assures all runtime registers are reset to their default values.

DOWNLOADING PROCESS

1. In order to make sure the device does not get reset during the downloading process assign a value to location 0x8000. This value will be compared to contents at this location at the end of the process.
2. Copy data from the runtime HEX file to RAM locations by stepping through addresses in the file using I^2C register command structure defined below:

Diagram Key

	Master to Slave
	Slave to Master
S	Start Condition
Sr	Repeated Start
Wr	Write (bit value of 0)
Rd	Read (bit value of 1)
A	Acknowledge (0=ACK, 1=NAK)
PEC	Packet Error Check
P	Stop Condition

Register Write

S	Slave Addr	Wr	A	Addr High	A	Addr Low	A	Data Byte	A	P
1	7	1	1	8	1	8	1	8	1	1

Register Write with PEC

S	Slave Addr	Wr	A	Addr High	A	Addr Low	A	Data Byte	A	PEC	A	P
1	7	1	1	8	1	8	1	8	1	8	1	1

Register Read

S	Slave Addr	Wr	A	Addr High	A	Addr Low	A	Sr	Slave Addr	Rd	A	Data Byte	A	P
1	7	1	1	8	1	8	1	1	7	1	1	8	1	1

Register Read with PEC																
S	Slave Addr	Wr	A	Addr High	A	Addr Low	A	Sr	Slave Addr	Rd	A	Data Byte	A	PEC	A	P
1	7	1	1	8	1	8	1	1	7	1	1	8	1	8	1	1

Note - per I^2C spec master NACKs after second read byte or PEC byte (if PEC used) to indicate to slave no more bytes expected and therefore the end of I^2C read transaction.

Note - I^2C register serial commands are structured differently than the system, power, IO and flash commands described in ANP-38.

3. Read the value at location 0x8000 and compare it to the value written in the step 1 above. If the value is different, the downloading process was not successful; the device shall be reset and the step 1 above repeated. Otherwise, the device has been configured correctly.
4. Set the chip ready high by sending a value of 0x0001 via the I^2C command **PWR_CHIP_READY** (0x0E) (refer to ANP-38).
5. If the configuration changes I^2C address of the device, make sure at this point to use the new address.

For assistance on how to communicate with devices covered in this document using I^2C commands, refer to ANP-38.

DOCUMENT REVISION HISTORY

Revision	Date	Description
1.0.0	04/08/2013	Initial Release of document, concurrent with PA5.02-r0
1.1.0	01/19/2014	Adding support for XRP7725, XRP9710/1 devices

FOR FURTHER ASSISTANCE

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