ANP-37

Power^{XR} EMI Reduction Technique Utilizing Spread-Spectrum Clock Dithering

July 2013 Rev. 1.0.1

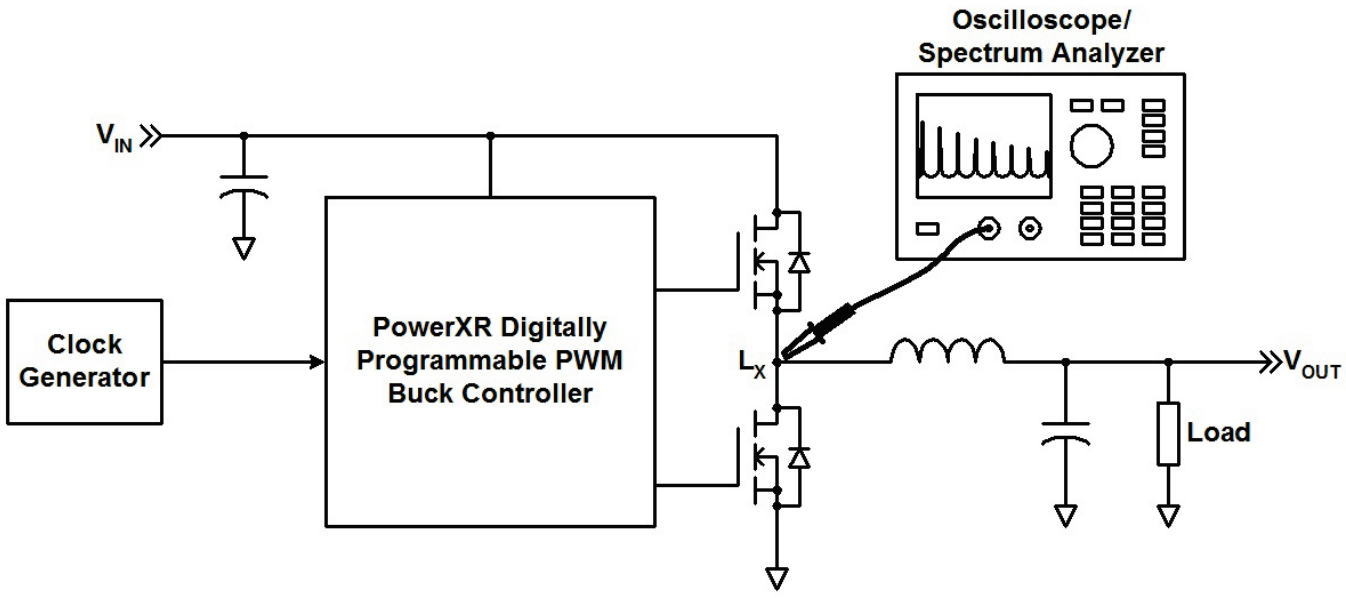
APPLICATION NOTE

GENERAL DESCRIPTION

It has been shown that the peak amplitudes of the spectral components contained within a PWM controller's EMI profile can be reduced by dithering the PWM controller's switching frequency. Clock dithering spread-spectrum techniques are not meant to replace traditional EMI-lowering techniques; however it can result in substantial reductions in the EMI profile of the system when used in conjunction with traditional techniques. It can also lower costs by reducing the amount of filtering and shielding needed to pass certain emissions standards. Exar Corporation's line-up of PowerXR devices allows the designer the flexibility to select a PWM controller switching frequency and to synchronize to an external clock source which can be dithered in order to employ this EMI lowering technique.

FEATURES

- **This application note applies to; XRP7704, XRP7708, XRP7713, XRP7714, and XRP7740**
- **Discusses theory behind spread-spectrum clock dithering and how it effects EMI**
- **Describes the PowerXR system under test**
- **System clock dithering using dedicated spread spectrum clock generators**
- **System clock dithering using FPGA devices**
- **Baseline and System Clock Dithering Emissions Data**



INTRODUCTION

Electromagnetic Interference (EMI) has long been an Achilles' heel when designing and qualifying electronic equipment. EMI is caused by the generation and radiation of undesirable electromagnetic energy and is emitted by any electronic system that has time varying voltages and currents. Since PWM controllers in power supply systems can have large time varying voltages and currents, they are prime candidates for generating undesirable EMI that may result in rather large peaks in the EMI profile (energy versus frequency) of the system. Sometimes, these undesirable peaks may cause the system to fail certain mandatory regulations set forth by agencies such as the FCC, CE and even the military. The most commonly utilized strategies to reduce EMI in power supplies having PWM controllers are larger input & output capacitors, chokes, coils, ferrite beads, feed-through capacitors, RC snubbers, multilayer circuit boards and even metalized shielding & gaskets. Other strategies that may be utilized which can have a negative impact on the overall efficiency of the power supply system include slowing down the turn-on and turn-off times of the high and low-side synchronous MOSFETs. One or more of these strategies may need to be employed in order to reduce emissions to acceptable levels and can often lead to very expensive and time consuming engineering efforts in addition to an increase in the bill of materials.

PowerXR is Exar Corporation's line-up of switching buck (step-down) Pulse-Width Modulated (PWM) controllers that are fully programmable over an I^2C interface and are available in both 3 and 4 channel versions. Both versions share similar features and capabilities and have integrated gate drivers capable of driving external MOSFETs that can support maximum output currents from 5A up to 15A or even greater. In addition to the PWM controllers, each device has an internal 100mA low drop-out linear regulator that can be programmed for either a 3.3V or 5V output to supply auxiliary or standby system power. Each channel has its own independent Digital Pulse-Width Modulator (DPWM) with 5 coefficient PID (Proportional-Integral-Differential) control that is fully programmable to tailor the control-loop response for PWM switching frequencies from 300kHz up to 1.5MHz. The PWM switching frequency is derived from either an internal oscillator or external system clock source both of which can range in frequency from 25.6MHz up to 48MHz. Many PWM controllers on the market today do not support synchronization to an external clock source; however the ability of the PowerXR devices to synchronize to this clock source makes it possible to implement a clock dithered, spread spectrum topology in order to reduce peaks in the EMI profile of the system.

The goal of the discussion which follows is to familiarize the reader with an EMI reduction technique that is often overlooked or not even considered due to the lack of available information. The undesirable peaks in the EMI profile of the system that result because of the PWM controller's switching frequency are made up of many components consisting of the fundamental switching frequency and the subsequent harmonics. Clock dithering and how it results in a spreading of the frequency spectrum of the emissions will be discussed followed by emissions data for both non-dithered and dithered clock signals for a typical PowerXR PWM controller circuit. Examples of dithered clock sources will then be discussed.

THEORY BEHIND SPREAD SPECTRUM SYSTEM CLOCK DITHERING & HOW IT AFFECTS EMI

A typical PWM controller switching frequency clock waveform and its resulting frequency spectrum is illustrated in Figure 1. Since this clock waveform is a pulse train and not a pure sinusoid, its frequency spectrum consists of the fundamental switching frequency, f_{sw}, and higher order odd harmonics. For example, if f_{sw}=300kHz, then the resulting higher order harmonics would be 900kHz, 1.5MHz, 2.1MHz, etc. The amplitude of the fundamental switching frequency will be the greatest with decreasing amplitudes of the higher order harmonics. The amplitudes of the actual radiated components will depend upon radiation transmission efficiencies and will depend on many factors including the

frequency, layout, trace lengths, etc. and is beyond the scope of this discussion; however, the amplitudes will generally decrease as the frequency increases with maybe one or more frequencies radiating more efficiently than others.

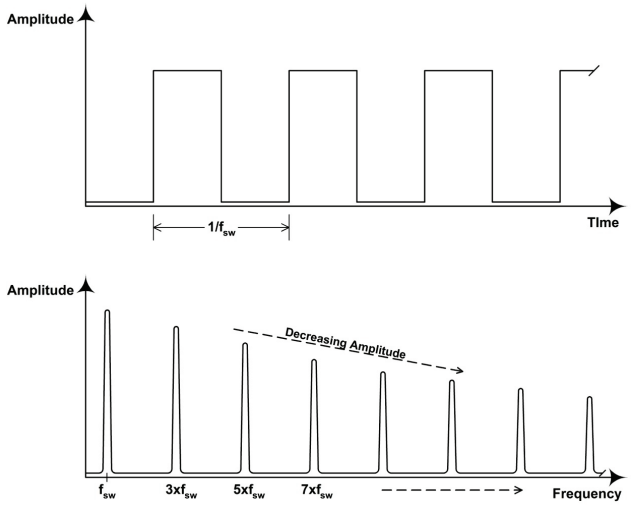


Figure 1 - Top: PWM Controller Switching Frequency Clock Waveform

Bottom: Resulting Frequency Spectrum

Spreading the spectrum of the fundamental switching frequency will distribute the concentrated energy contained in the fundamental frequency and the higher order harmonics over a wider bandwidth, thereby reducing peak emissions. This method of modulating the fundamental switching frequency between two frequency boundaries is referred to as clock dithering. Dithering of the PWM controller's switching frequency will vary the fundamental switching frequency over a narrow range. For example, if f_{SW}=300kHz, then a ±1.5% symmetrical dithering about this frequency (referred to as center-dithering) will result in a range of PWM controller switching frequencies from 295.5kHz up to 304.5kHz. The resulting PWM controller switching frequency clock waveform and its resulting frequency spectrum is illustrated in Figure 2. Since it would be difficult to illustrate the dithered clock in the traditional Amplitude vs. Time format, the format chosen for illustrative purposes is a Frequency vs. Time distribution curve. The frequency modulation chosen for this illustration follows a triangle-shaped waveform. Other modulating waveforms are possible, but it has been shown in the literature that the simple triangle waveform yields the best results. Notice that the resulting dithered frequency spectrum shows a decrease in the amplitudes of the components and an increase in their individual bandwidths. There has also been an increase in the noise floor because the wideband energy remains constant. The dither frequency, f_{DITHER}, is typically between 20kHz and 60kHz.

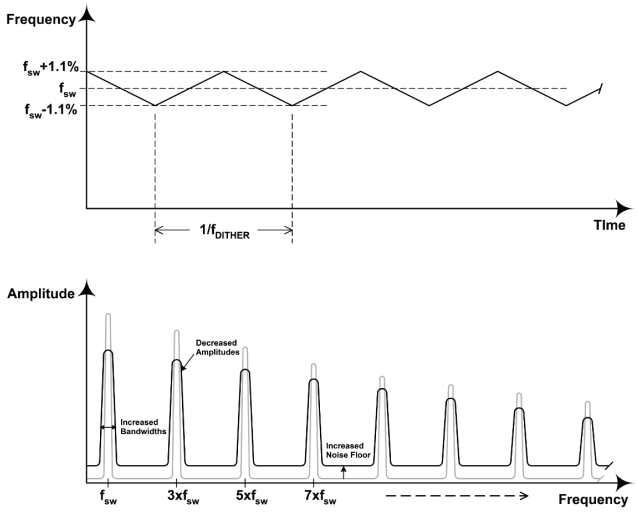


Figure 2 - Top: Dithered PWM Controller Switching Frequency Clock Distribution

Bottom: Resulting Frequency Spectrum (Non-Dithered Spectrum Also Shown)

It has been shown in the literature that the reduction in amplitude (in dB) of the spectral components as a result of clock dithering is given by,

$$SpectralAttenuation\ [dB]=10*\log[(f_{SW}*\delta)/(f_{DITHER}/n)]$$

where,

f_{SW}=PWM Controller Switching Frequency (between 300kHz and 1.5MHz for PowerXR devices)

δ=Percentage Dither about the Fundamental Switching Frequency (typically between ±0.25% and ±5%)

f_{DITHER}=Dither Modulation Rate (typically between 20kHz and 60kHz)

n=PowerXR System Clock Frequency Divider (see Table 1)

An increase in δ has the same effect as a decrease in f_{DITHER}. Before considering an example, it is necessary to understand the PowerXR requirements with respect to synchronization to an external clock source. PowerXR utilizes a programmable system clock frequency and a programmable divider to generate the PWM controller switching frequency, f_{SW}. When a PowerXR device is configured to operate from an external synchronizing clock source, the frequency of the source must be within ±5% of the internal system clock frequency as set forth in Table 1. Because of this requirement, f_{DITHER} should be kept below ±5% (±4% max is recommended). As an example, if the PowerXR device is configured to operate at a PWM controller switching frequency of 300kHz, then one of the two possible selections in Table 1 which will yield this PWM controller switching frequency is when the system clock frequency is 28.8 MHz and the system clock frequency divider, n, is 96. Using this as an example in calculating the expected spectral attenuation for δ=±1.1% (2.2%) and f_{DITHER}=56kHz yields,

Spectral Attenuation=$10*\log[(f_{sw}*\delta)/(f_{DITHER}/n)]$
$=10*\log[(300kHz)*(0.022)/(56kHz/96)$
$=-10.5dB$

System Clock Frequency							
48 MHz	44.8 MHz	41.6 MHz	38.4 MHz	35.2 MHz	32 MHz	28.8 MHz	25.6 MHz
fsw=1.5 MHz **n=32**	fsw=1.4 MHz **n=32**	fsw=1.3 MHz **n=32**	fsw=1.2 MHz **n=32**	fsw=1.1 MHz **n=32**	fsw=1.0 MHz **n=32**	fsw=900 kHz **n=32**	fsw=800 kHz **n=32**
fsw=1.0 MHz **n=48**	fsw=933 kHz **n=48**	fsw=867 kHz **n=48**	fsw=800 kHz **n=48**	fsw=733 kHz **n=48**	fsw=667 kHz **n=48**	fsw=600 kHz **n=48**	fsw=533 kHz **n=48**
fsw=750 kHz **n=64**	fsw=700 kHz **n=64**	fsw=650 kHz **n=64**	fsw=600 kHz **n=64**	fsw= 550kHz **n=64**	fsw=500 kHz **n=64**	fsw=450 kHz **n=64**	fsw=400 kHz **n=64**
fsw=600 kHz **n=80**	fsw=560 kHz **n=80**	fsw=520 kHz **n=80**	fsw=480 kHz **n=80**	fsw=440 kHz **n=80**	fsw=400 kHz **n=80**	fsw=360 kHz **n=80**	fsw=320 kHz **n=80**
fsw=500 kHz **n=96**	fsw=467 kHz **n=96**	fsw=433 kHz **n=96**	fsw=400 kHz **n=96**	fsw=367 kHz **n=96**	fsw=333 kHz **n=96**	fsw=300 kHz **n=96**	
fsw=429 kHz **n=112**	fsw=400 kHz **n=112**	fsw=370 kHz **n=112**	fsw=343 kHz **n=112**	fsw=314 kHz **n=112**			
fsw=375 kHz **n=128**	fsw=350 kHz **n=128**	fsw=325 kHz **n=128**	fsw=300 kHz **n=128**				

Table 1 – PowerXR System Clock Frequency Dividers, n

In this example, the amplitude of the fundamental in addition to all of the harmonics will be attenuated by about 10.5dB.

PowerXR System Device Under Test

The test setup used to gather emissions data for both non-dithered and dithered clock sources is shown in Figure 3. The PowerXR device is configured to synchronize to the external clock source supplied by the Clock Generator block. The L_X node in the circuit is the measurement point for collection of non-dithered and dithered emissions data since it

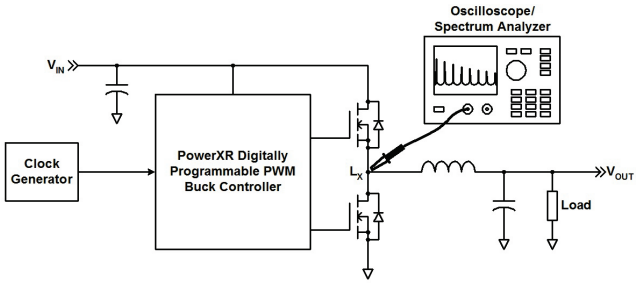


Figure 3 - Test Setup

contains the highest voltage peaks and all of the relevant radiated spectral components. Keep in mind that data gathered at the L_X node is not the actual radiated emissions data because it does not include the radiation efficiencies for each spectral component, but it can be used to compare relative levels between the non-dithered and dithered clock data.

A detailed circuit schematic containing the XRP7714 PowerXR device is shown in Figure 5. The XRP7714 is a 4-channel digital PWM buck controller; however, for clarity, only components and connections for channel 1 are shown, and only channel 1 was enabled and used to gather emissions data. The external synchronizing clock source comes in through GPIO1, and the XRP7714 is configured over the I^2C interface through GPIO4 and GPIO5. The L_X node measurement point is labeled as LX1 on the schematic. Notice that the circuit contains an RC snubber network from the L_X node to ground and small resistor values in series with the gates of the high and low-side synchronous MOSFETs. These are commonly employed EMI reduction techniques because the snubber network helps to reduce ringing at the L_X node, and the series gate resistors slow down the turn-on and turn-off times of the MOSFETs (at the expense of efficiency).

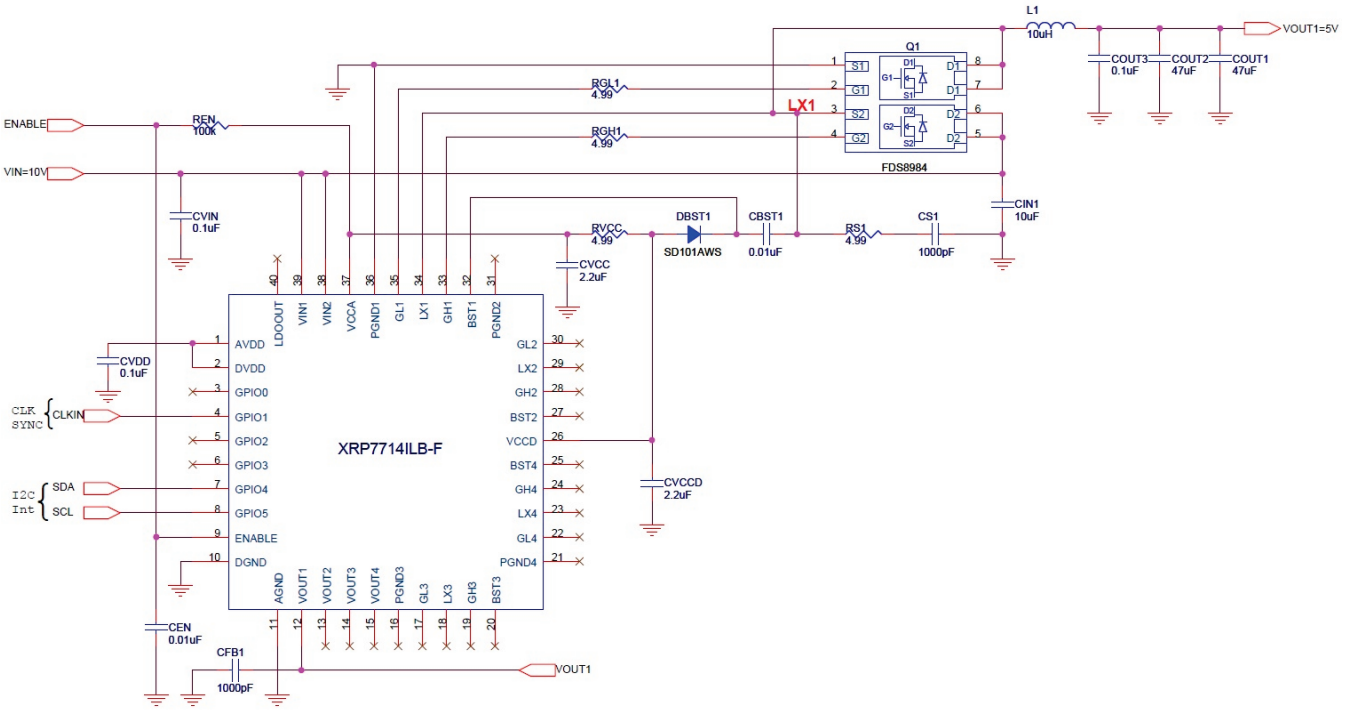


Figure 5 - PowerXR Circuit Schematic

The PowerXR devices are configured over the I^{2}C port using the PowerArchitect development software which is available for download from Exar's website. The XRP7714 device was configured for a PWM switching frequency of 300kHz as shown in Figure 4 with a resulting internal System Clock Frequency of 28.8MHz. The device was also configured for synchronization to an external clock source as shown in Figure 6. Notice that "Auto switch back to Internal Oscillator" was chosen which allows the XRP7714 to operate from the internal System Clock Frequency in the event of the absence of the external clock source. Also, notice that the input voltage was chosen to be 10V, and the output voltage was chosen to be 5V in order to achieve a 50% positive duty cycle of the switching waveform appearing at the Lx node. This was purposely done, so the frequency spectrum will contain only the odd order harmonics as previously illustrated in Figure 1. Duty cycles other than 50% will result in a more complex frequency spectrum containing harmonics that are integer multiples of the fundamental switching frequency. In order for the XRP7714 to synchronize to the external clock source, it must fall within ±5% of the internal System Clock Frequency of 28.8MHz as shown in the data sheet excerpt in Figure 7.

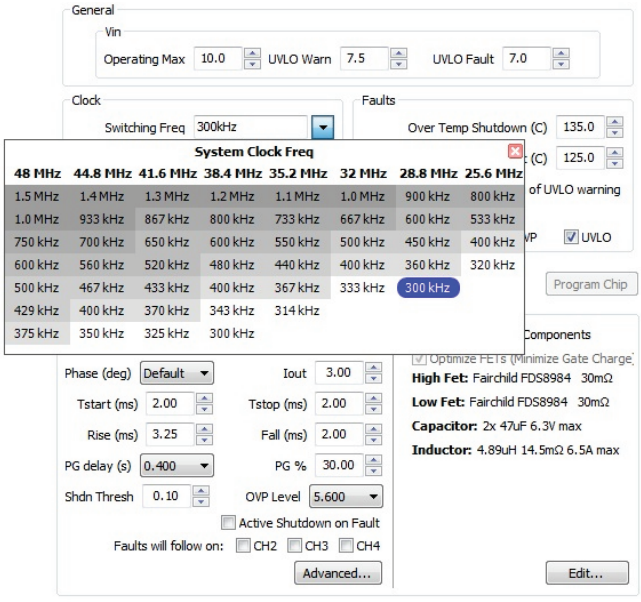


Figure 4 - "Power Design" Screenshot From PowerArchitect Design Software

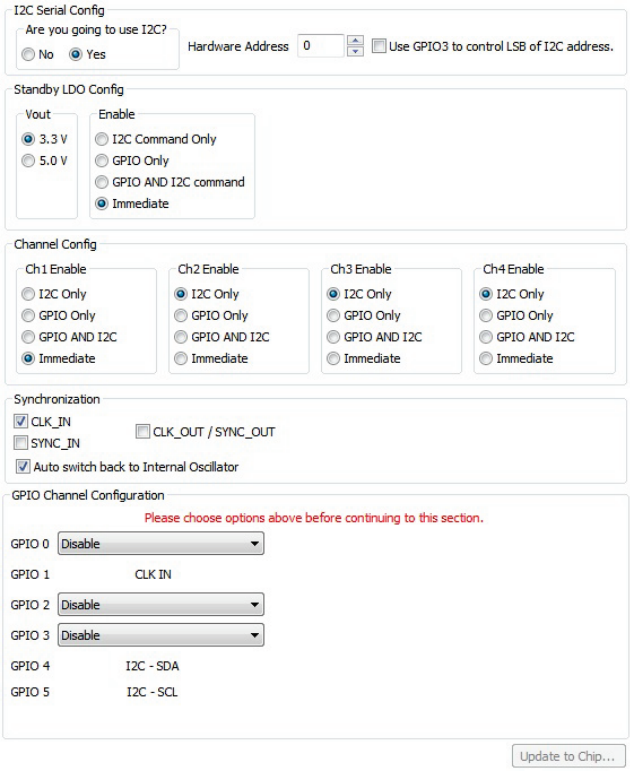


Figure 6 - "Digital Design" Screenshot From PowerArchitect Design Software.

ELECTRICAL SPECIFICATIONS

Specifications with standard type are for an Operating Junction Temperature of T_J = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, VIN_1 = 4.75V to 25V, VIN_2 = 4.75V to 25V.

PWM Generators and Oscillator

Parameter	Min.	Typ.	Max.	Units		Conditions
CLOCK IN Synchronization Range	-5		5	%	•	

Figure 7 - XRP7714 Synchronizing Clock Source Requirement (From Data Sheet)

System Clock Dithering Using Dedicated Spread Spectrum Clock Generators

Several manufacturers produce dedicated IC clock dithering spread-spectrum clock generators. A typical block diagram is shown in Figure 8. The reference clock source for the IC is either derived from an external crystal (XTAL) or an external clock source (CLKIN). The programmable PLL typically generates a clock source in the range from a few MHz up to over 100MHz depending on the crystal or external clock source frequency. Several external spread-spectrum control lines are usually available to control the range of dithering relative to the reference clock source frequency. These control lines may also determine if the clock spectrum will be center-dithered, down-dithered or up-dithered relative to the reference clock source frequency. The exact range of reference frequencies supported will depend on the IC, but it usually covers a range broad enough to support the required PowerXR system clock frequencies discussed earlier. There are also many manufacturers of crystals, so it is usually straight forward to find one close in frequency to the required PowerXR system clock frequency. For example, if the required PowerXR system clock frequency is 28.8MHz (300kHz PWM switching frequency), then a suitable crystal might be the Abracon ABLS 28.63636MHz-B4-F-T which has a frequency of 28.63636MHz which is within 0.57% of the PowerXR system clock frequency of 28.8MHz. For example, this would also allow for a center-dithering of ±1.1% (with a comfortable margin) about the reference clock source frequency without violating the PowerXR external clock synchronization requirement which requires it to fall within ±5% of its internal system clock frequency which, in this example, is 28.8MHz.

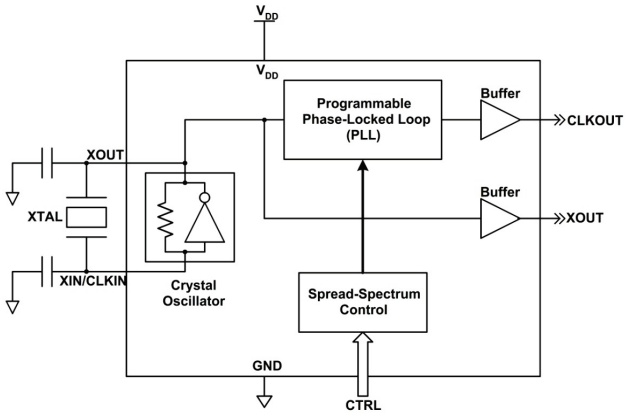


Figure 8 - Dedicated IC Spread Spectrum Clock Generator Block Diagram

System Clock Dithering Using FPGA Devices

A detailed treatise of how to implement a spread-spectrum clock generator using an FPGA device is beyond the scope of this discussion; however, it is beneficial to provide a brief overview. Detailed information on implementing a spread-spectrum clock generator can be obtained from the FPGA

manufacturer. If FPGA resources are present and available in the system, then implementation of the spread-spectrum clock generator in the FPGA can provide cost and space savings over the dedicated IC approach discussed earlier.

A typical block diagram of a spread-spectrum clock generator implemented with an FPGA device is shown in Figure 9. Most FPGA manufactures provide spread-spectrum building blocks or primitives that can be used to generate a clock-dithered signal from a reference clock source. The Reference Clock is typically derived from a divider or multiplier block and is equal in frequency to the required PowerXR system clock frequency. The Fine Tuner Block is controlled by the Tuning/Dithering Command Block and ramps the PLL output frequency (CLKOUT) up and down with configurable frequency steps and configurable time intervals between these steps. Configuration details of the PLL Core Block can be obtained from the FPGA manufacturer, but the internal feedback is typically broken and the Fine Tuner Block is placed within the External Feedback loop as shown.

Implementation of the spread-spectrum clock generator in the FPGA is only possible if there are enough available logic and routing resources after implementation of other system resources for which the FPGA was originally intended. If it is anticipated that EMI will be an issue in the overall system, then proper selection of an FPGA device (or devices) and partitioning of FPGA resources can help alleviate any allocation issues that might arise.

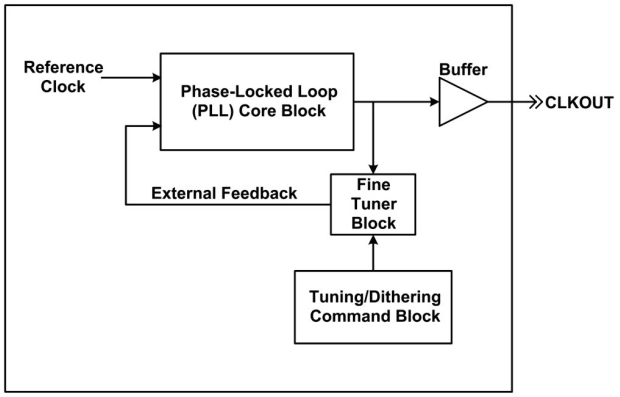
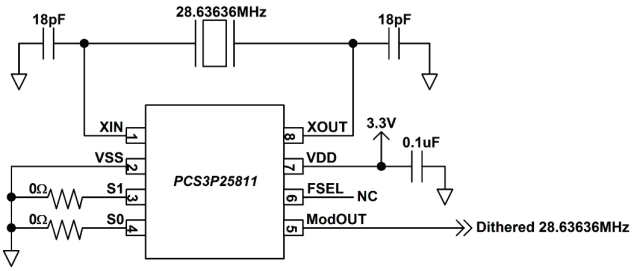


Figure 9 - FPGA Spread Spectrum Clock Generator Block Diagram

BASELINE & SYSTEM CLOCK DITHERED EMISSIONS DATA

The PCS3P25811 spread-spectrum clock generator was used as the clock generator source for the baseline (no spreading/dithering) and system clock dithered emissions data. A schematic is shown in Figure 10. Baseline emissions data was gathered using the 28.63636MHz ModOUT clock source with the 0Ω jumpers removed (no spreading) and then the 0Ω jumpers were installed, and clock-dithered emissions data was gathered using the dithered ModOUT. ±1.1% center spreading was achieved with the 0Ω jumpers installed at a dither modulation rate of,

28.63636MHz/512=55.93kHz≈56kHz.



CLKIN (MHz)	FSEL	S1=0, S0=0	S1=NC, S0=NC	Modulation Rate
28-32	NC	±1.1%, Center Spread	No Spread	XTAL Frequency/512

Figure 10 - Spread Spectrum Clock Generator Schematic

The range of dithered frequencies for a 28.63636MHz ±1.1% dithered clock source are found as,

f_{max}=(28.63636MHz)(1.011)/n
=(28.63636MHz)(1.011)/96
=301.6kHz

f_{nom}=28.63636MHz/n
=28.63636MHz/96
=298.3kHz

f_{min}=(28.63636MHz)(1-0.011)/n
=(28.63636MHz)(1-0.011)/96
=295.0kHz

where f_{nom} is the baseline (no spreading) frequency, and n=96 is the PowerXR System Clock Frequency Divider as discussed earlier. Figure 11 is a scope plot which illustrates this range of frequencies as measured at the switch node (LX1). f_{max} was measured as 301.5KHz (Ref1), and f_{min} was measured as 295.3kHz (Ref3). This represents a frequency spreading of +1.07%/-1.01% (2.08%) which is in very close agreement with the expected spread of ±1.1% (2.2%). The baseline frequency was measured as f_{nom}=295.3kHz (CH1) as expected. Also, notice that duty cycles of each waveform are about 50% as predicted by the voltage conversion ratio of V_{OUT1}/V_{IN}=5V/10V=0.5.

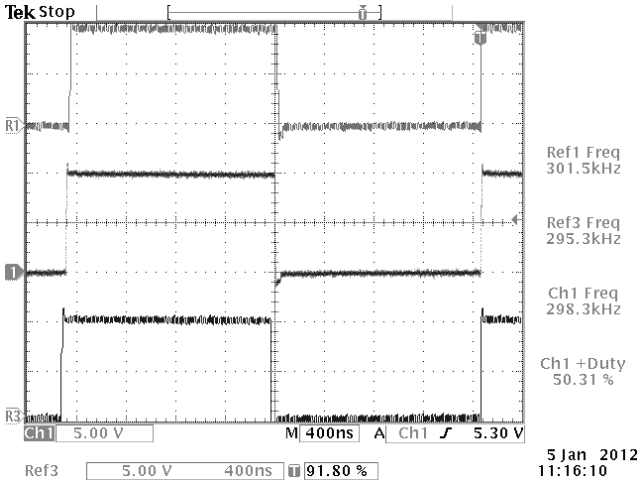


Figure 11 - Switch Node (LX1) Waveforms Illustrating Range of Dithered Frequencies

The baseline (no spreading) frequency spectrum as measured at the switch node (LX1) is shown in Figure 12, and the resulting dithered frequency spectrum is shown in Figure 13. An overlay of these two spectrums is shown in Figure 14 which makes it easier to compare the two. The frequency band shown in these figures is between 6.50MHz and 9.00MHz. Limitations of the oscilloscope's noise floor capabilities prevent accurate measurements at higher frequencies, but these plots serve as good representations of the expected behavior at other frequencies. The FFT (Fast Fourier Transform) function built into the oscilloscope has limitations and results in some distortions of the amplitudes, widths and overall shapes of the frequency spectrum components, but it still serves to illustrate the advantages of the frequency dithering technique very well. Notice the amplitudes of all of the dithered frequency spectral components are significantly lower than the corresponding baseline components and that their widths are also slightly greater. The overall noise floor of the dithered spectrum is also slightly higher, but limitations of the oscilloscope's noise floor capabilities prevent this from being seen in these plots. The low amplitude spectral components between the larger main spectral components are the result of the duty cycle not being exactly 50%. When a time domain pulse train has a duty cycle of exactly 50%, the resulting higher order spectral components are odd multiples of the fundamental frequency, and for duty cycles other than 50%, the resulting spectral components are integer multiples of the fundamental frequency.

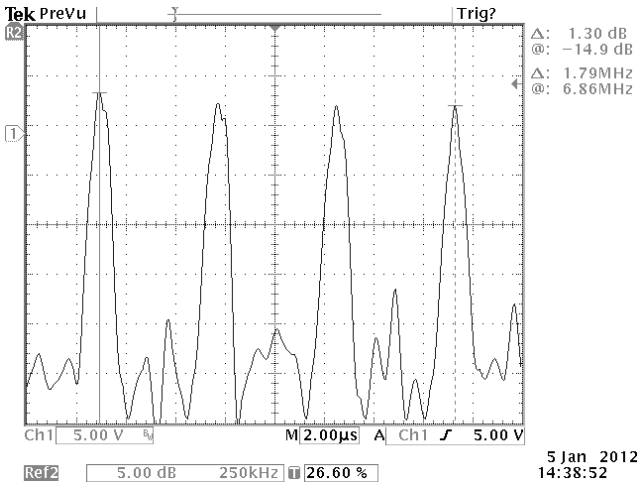


Figure 12 - Baseline (No Spreading) Frequency Spectrum at Switch Node (LX1)

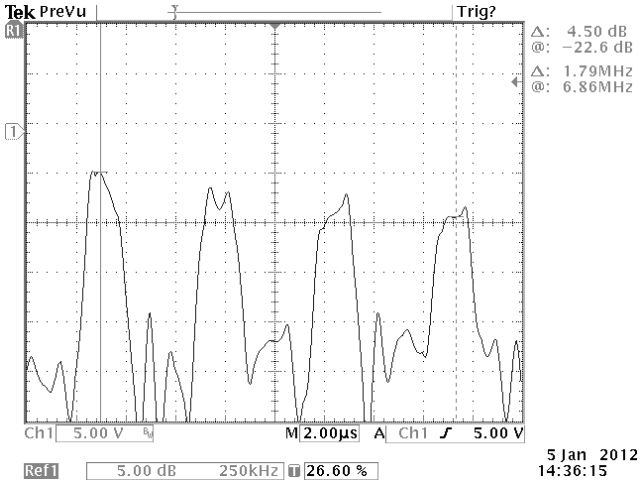


Figure 13 - Dithered (with Spreading) Frequency Spectrum at Switch Node (LX1)

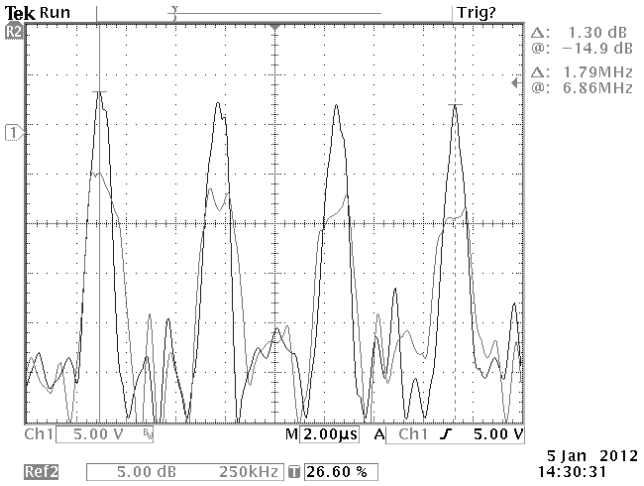


Figure 14 - Overlay of Baseline and Dithered Frequency Spectrums at Switch Node (LX1)

The table in Figure 15 summarizes the results of these measured frequency spectrums. Notice that the separation in frequency for each of the spectral components is approximately 2(300kHz)=600kHz as expected since each spectral component is an odd multiple (3, 5, 7, 9, etc.) of the fundamental frequency which is approximately 300kHz. The expected reduction in amplitudes of the frequency spectrum components was shown earlier to be approximately 10.5dB, so these results are in fairly good agreement with theory. Differences between measurements and theory can most likely be attributed to errors introduced by limitations of the oscilloscope and the FFT function and the difference between the expected frequency spreading of ±1.1% (2.2%) and the actual measured spreading of +1.07%/-1.01% (2.08%). Taking into consideration the actual measured spread of 2.08%, the actual fundamental switching frequency of 298.3KHz and the actual dithered modulation rate of 55.93kHz, the Spectral Attenuation is found as,

$$SpectralAttenuation=10*\log[(f_{sw}*\delta)/(f_{DITHER}/n)]$$
$$=10*\log[(298.3kHz)*(0.0208)/(\ 55.93kHz/96)$$
$$=-10.3dB$$

This only accounts for a small portion of the error, so the remaining error is most likely attributed to limitations of the oscilloscope and the FFT function. More precise results could have been obtained by taking the measurements with a dedicated spectrum analyzer.

Frequency	Amplitude		Amplitude Reduction
	Non-Dithered	Dithered	
6.86MHz	-14.9dBVrms	-22.6dBVrms	7.7dBVrms
7.46MHz	-16.0dBVrms	-24.2dBVrms	8.2dBVrms
8.05MHz	-16.2dBVrms	-24.8dBVrms	8.6dBVrms
8.65MHz	-16.2dBVrms	-26.2dBVrms	10.0dBVrms

Figure 15 - Summary of Non-Dithered and Dithered Frequency Spectrums

CONCLUSIONS

It has been shown that the peak amplitudes of the spectral components contained within a PWM controller's EMI profile can be reduced by dithering the PWM controller's switching frequency. Clock dithering spread-spectrum techniques are not meant to replace traditional EMI-lowering techniques; however it can result in substantial reductions in the EMI profile of the system when used in conjunction with traditional techniques. It can also lower costs by reducing the amount of filtering and shielding needed to pass certain emissions standards. Exar Corporation's line-up of PowerXR devices allows the designer the flexibility to select a PWM controller switching frequency and to synchronize to an external clock source which can be dithered in order to employ this EMI lowering technique. External spread-spectrum dithered clock sources discussed were dedicated integrated circuits and FPGAs. The FPGA clock source is the best choice when it is already available in the system since it eliminates the need for having to add additional components, and the dedicated integrated circuit solution is required when an FPGA is not available.

DOCUMENT REVISION HISTORY

Revision	Date	Description
1.0.0	07/22/2013	Initial release of document
1.0.1	07/29/2013	Corrected Figure Captions and reformatted

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48720 Kato Road
Fremont, CA 94538 – USA
Tel.: +1 (510) 668-7000
Fax: +1 (510) 668-7030
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