

ENVISIONING • EMPOWERING • EXCELLING



**XR224xx**  
**USB Hubs**  
Design Guide

## Revision History

Document No.	Release Date	Change Description
203DGR00	4/20/20	Initial release.

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## Introduction

The XR224xx Design Guide a helpful checklist of schematic design and PCB layout tips to aid in applying a XR224xx USB Hub to your PCB design. The XR224xx Family are USB 2.0 4-port and 7-port hub controllers. The XR22404 4-port hub can be configured for downstream device charging and is compatible with Battery Charging specification revision 1.1/1.2.

Please refer to the respective XR224xx Data Sheet for more information.

## Reference Documentation

[XR22404](#) Data Sheet

[XR22414](#) Data Sheet

[XR22417](#) Data Sheet

Visit [www.maxlinear.com](http://www.maxlinear.com) to obtain copies of these documents.

## Pin Groups

The tables below are arranged by the following pin groups:

- USB Upstream Port
- USB Downstream Ports
- USB Hub other "Special Handling" Device Pins
- Voltage Rails
- General PCB Layout

## Design and Layout Recommendations

**Table 1: USB Upstream Port**

Schematic Design Recommendations
Ensure there are no external components on <b>USBD+ / USB-</b> unless tested in compliance with the USB 2.0 spec. For example, no series resistance, inductance or capacitance. No shunt capacitance. Exceptions are ESD protection diodes, EMI filters that have demonstrated compliance with USB 2.0 high speed signaling.
Layout Recommendations
<b>USBD+ / USB-</b> are high speed USB signaling at 480MHz. Ensure 90Ω differential impedance.
<b>USBD+ / USB-</b> should not be routed over a split reference plane.
<b>USBD+ / USB-</b> should be length matched, ideally to within ±20 mils.
<b>USBD+ / USB-</b> should have no greater than 2 vias.
<b>USBD+ / USB-</b> should have no stubs on these traces greater than 200 mils, for example to test points.

**Table 2: USB Downstream Ports**

Design and Layout Recommendations
All downstream ports of the USB hubs may operate at high, full or low speed, depending on the speed of the attached device. All notes regarding the USB upstream port should also be followed by all downstream port USB data signals.

**Table 3: USB Hub "Special Handling" Device Pins**

Schematic Design Recommendations
Connect <b>VBUS_SENSE</b> , using pin description in the Data Sheet, with voltage divider from USB host VBUS power input. Required for proper operation in self-powered USB designs.
For USB suspend mode power compliance, use the <b>LOW_PWR#</b> output to power down other devices powered by USB VBUS.
Layout Recommendations
Connect <b>XTAL</b> pins with short traces isolated from other high frequency nets.
Connect <b>REXT</b> with short trace.
Use power plane, partial power plane or heavy power trace to connect <b>3V3_OUT</b> to VCC33 pins when powered by 5V V <sub>CC</sub> .
Use power plane, partial power plane or heavy power trace to connect <b>1V8_OUT</b> to VCC18 pins.

**Table 4: Voltage Rails**

Schematic Design Recommendations
An in-rush current limiting circuit is recommended (refer to XR224xx Evaluation board schematics) to meet USB compliance.
All decoupling capacitors should be implemented without traces to power or ground rails if possible.
Bulk decoupling:
USB requires between 1 and 10uF of bulk capacitance on the VBUS power rail from the USB host. We recommend 4.7uF. In general if no in-rush current limiting circuit is used, a tantalum capacitor is recommend except for embedded applications or applications where no external USB cable will be used. For all other voltage rails (including any external V <sub>CC</sub> supply voltages to the XR224xx device in self-powered mode) a minimum of 10uF of bulk decoupling should be used.
High frequency decoupling:
For all designs, a 100nF high frequency decoupling capacitor is recommended on each power pin, located as close as possible to the device power pin.

**Table 5: General PCB Layout****Layout Recommendations**

A minimum of a 4 layer PCB is critical with 5V or 3.3V power and ground reference planes (2 and 3) and microstrip signal layers (layers 1 and 4).



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